

**ANALOG AND MIXED-SIGNAL CHIP DESIGN GETS MORE PRODUCTIVE WITH  
TANNER EDA'S NEW S-EDIT SCHEMATIC CAPTURE TOOL**

**Fully User Programmable Design Capture Tool Tightly Integrated with Simulation;  
Provides Complete Design Flow from Design to Verification**

**MONROVIA, Calif., March 8, 2006** – Tanner EDA, which provides cost-effective and easy-to-use tools for the design of mixed-signal and analog circuits, today announced its new S-Edit design environment for schematic capture. For the first time, users can get an integrated suite of affordable Tanner analog and mixed-signal design capture, simulation, layout, design rule checking and verification tools. S-Edit also supports legacy tools and data to preserve existing investments.

S-Edit is anticipated to reduce front-end design time, which typically is about 60 percent of the total design process. For example, S-Edit supports physical design from T-cells, which automatically generates the design and tracks its status. Once a design is completed, modifying it or creating next-generation devices is much faster than in previously available analog or mixed-signal design tools. To further simplify and shorten the design process, S-Edit also imports schematics from Cadence and ViewDraw tools.

“For most analog and mixed-signal designers and their management, the key issue for tools is buying expensive ones versus spending time to build proprietary ones,” said Mass Sivilotti, chief scientist, Tanner Research. “S-Edit gives these designers a cost-effective, productive option to front-end design so they can use their existing design flow from Tanner EDA or with other tools.”

Tight integration with Tanner’s T-Spice analog simulation tool and W-Edit waveform probing tool enables designers to move quickly through the design flow. Designers can take the designs created in S-Edit and use Tanner’s L-Edit and verification tools to finalize the process. A Windows-based user interface is common to all Tanner tools, meaning designers can get started in minutes and work easily across tools. User interfaces can be localized as well.

**S-Edit Features**

S-Edit provides schematic capture, netlist input and output with automatic conversion of Cadence® and ViewDraw® EDIF schematics, and integrated analog simulation. Users can run simulations and cross-probe from within S-Edit, making design more efficient and real-time. Other key features include:

- Viewing of operating point simulation results directly on the schematic
- Exporting of SPICE, EDIF, Verilog, and VHDL

- Advanced array support
- Buses and port bundles
- Rubberband connectivity editing
- Viewing of evaluated results of any calculated parameters
- Multiple symbol, schematic, and interface views per cell
- Multiple library support
- Schematic ERC checker
- Integrated symbol editor and library browsers
- Fully scriptable and expandable using TCL command language
- Rapid recovery from network or hardware failure via a replayable log file
- Available in node- and network-locked licenses

For more details on S-Edit features, go to [www.tannereda.com](http://www.tannereda.com).

#### **Availability and Pricing**

S-Edit is available now with pricing starting at US\$3,500. For further pricing information, contact Tanner EDA sales at [sales@tanner.com](mailto:sales@tanner.com) or call 1-877-325-2223.

#### **About Tanner EDA**

Tanner EDA is a leading provider of easy-to-use, PC-based electronic design automation (EDA) software solutions for the design, layout and verification of analog/mixed-signal integrated circuits, ASICs and MEMS. Its solutions help speed designs from concept to silicon and are used by thousands of companies to develop devices cost-effectively in the biomedical, consumer electronics, next-generation wireless, imaging, power management and RF market segments. Founded in 1988, Tanner EDA is a division of privately held Tanner Research, Inc. For more information, go to [www.tannereda.com](http://www.tannereda.com).