

New Features in Tanner EDA v15.10

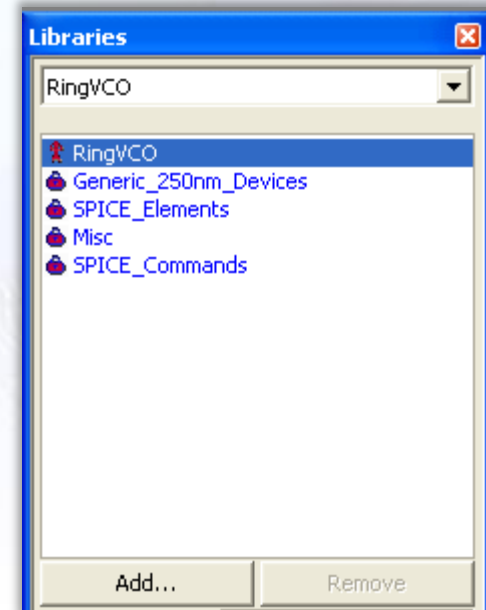
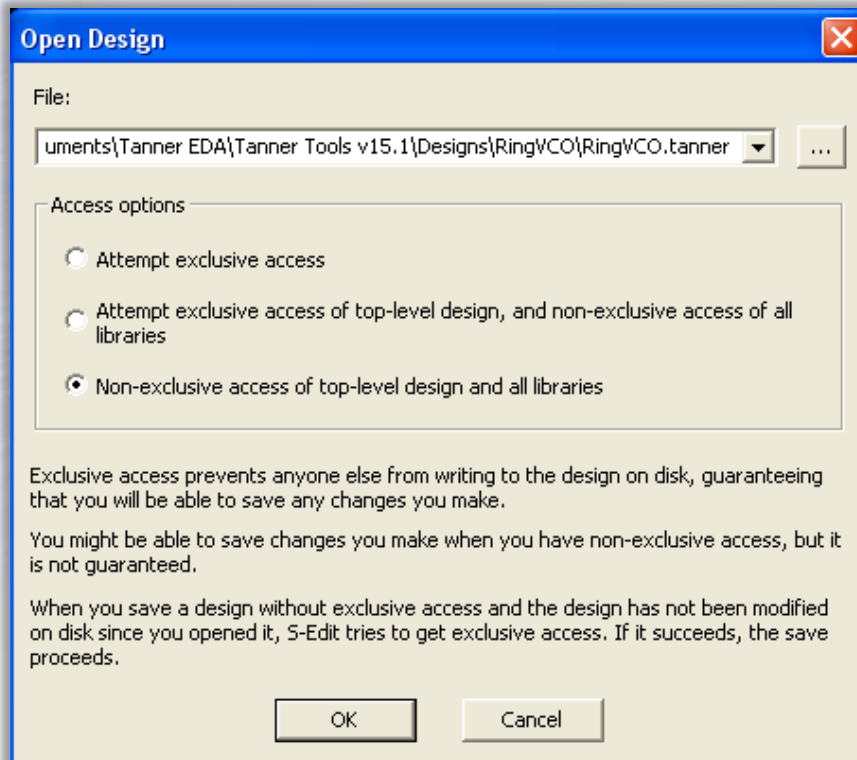
December 2010

Tanner EDA v15.10 New Feature Summary

- S-Edit
 - Library Write Access Enhancements
 - Improved Bus, Port, and Netname Processing
 - Spice Hierarchical Netlist Import
 - Additional Corner Simulation Settings
 - Addition of Monte Carlo Simulation Settings
- W-Edit
 - New Histogram Chart
 - New Eye Diagrams
 - New Chart Style Setup
 - Copy to Clipboard or Save Charts as Windows Metafiles *.wmf
 - Import/Export of Traces from/to a File or Clipboard
- T-Spice
 - Improved Performance
 - Updated Models
 - Simulation Files/Folders Can Now be Easily Renamed
- L-Edit
 - Improved Wire Drawing With Vias
 - Snap to Intersection
 - SDL Jump to Schematic
- HiPer Verify
 - DRC / Extract Speed Improvement
- HiPer DevGen
 - Added Resistor Arrays

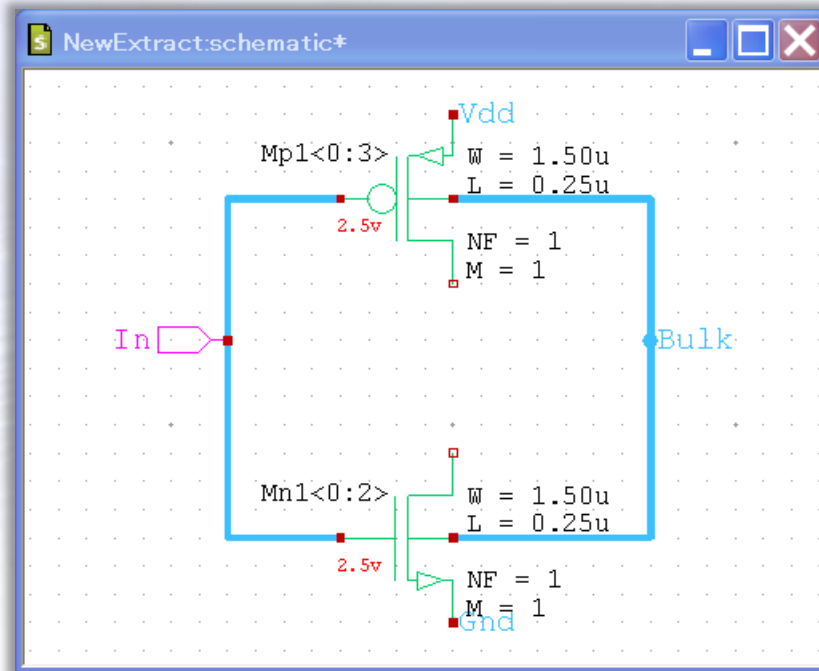
S-Edit: Library Write Access Enhancements

- Improved control over write permissions allows users to choose to open a design with Exclusive or Non-Exclusive access
- Opening a design with Exclusive Access reserves the right to save a design, so that no-one else can write to it while you have it open. This “write reservation” gives you the exclusive right to save a design
- Opening a design with Non-Exclusive Access means you might be able to write to the design in the future, as long as no one else secures a write reservation before you attempt to save the design



S-Edit: Improved Bus, Port, and Netname Processing

- If multiple buses (with different dimensions) connect to a single net, S-Edit will now connect all the buses to this single net
 - Prior to v15.10 this would be an error due to the connection of busses with different dimensions



```
NewExtract.sp
*----- Devices With SPICE.ORD
***** Top Level *****
MMn1<0> N_1 In Gnd Bulk NMOS25
MMn1<1> N_2 In Gnd Bulk NMOS25
MMn1<2> N_3 In Gnd Bulk NMOS25
MMp1<0> N_4 In Vdd Bulk PMOS25
MMp1<1> N_5 In Vdd Bulk PMOS25
MMp1<2> N_6 In Vdd Bulk PMOS25
MMp1<3> N_7 In Vdd Bulk PMOS25
```

S-Edit: Spice Hierarchical Netlist Import

- Spice, Verilog and EDIF import will now create SPICE Text views.
 - Spice views will be now saved with the design
- Importing a hierarchical netlist will create separate cells for each subcircuit in the netlist

```
RingWCO_TestBench.sp *
* Organization: Tanner EDA - Tanner Research, Inc.
* Info: Testbench for RingWCO
* Date: 12/20/2010 5:56:19 AM
* Revision: 63 $ $x=7600 $y=600 $w=3600 $h=1200
***** Subcircuits *****
.subckt Control VTune Vb1 Vb2 Vbias Gnd Vdd

MM5n N_2 N_2 Vbias 0 NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u $ $x=3907 $y=3400
+$h=600 $m
MM6n Vb2 N_2 N_3 0 NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4893 $y=3400 $w
+$h=600
MM7n N_3 VTune Gnd 0 NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u $ $x=5307 $y=2700
+$h=600 $m
MM1p N_1 Vb1 Vdd Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=3907 $y=500
+$h=600 $m
MM2p Vb1 Vb1 Vdd Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=4893 $y=500
+$h=600
MM3p N_2 Vb2 N_1 Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=3907 $y=420
+$h=600 $m
MM4p Vb2 Vb2 Vb1 Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=4893 $y=420
+$h=600
.ends

.subckt DiffCell Inm Inp Outm Outp VTune Vb1 Vb2 Gnd Vdd W=5.00u

MN1 Outm VTune Gnd Gnd NMOS25 W=1.5u L=2u M=1 AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4007 $y=2600
+$h=600 $m
MN2 Outp VTune Gnd Gnd NMOS25 W=1.5u L=2u M=1 AS=975f PS=4.3u AD=975f PD=4.3u $ $x=4993 $y=2600
+$h=600
MP1 N_1 Vb1 Vdd Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=4293 $y=5100
+$h=600
MP2 N_2 Vb2 N_1 Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u $ $x=4293 $y=4400
+$h=600
MP3 Outm Inp N_2 Vdd PMOS25 W=W L=250n M=1 AS='650n*W' PS='1.3u+2*W' AD='650n*W' PD='1.3u+2*W' $
+$y=3600 $w=414 $h=600
MP4 Outp Inm N_2 Vdd PMOS25 W=W L=250n M=1 AS='650n*W' PS='1.3u+2*W' AD='650n*W' PD='1.3u+2*W' $
+$y=3600 $w=414 $h=600 $m
.ends
```

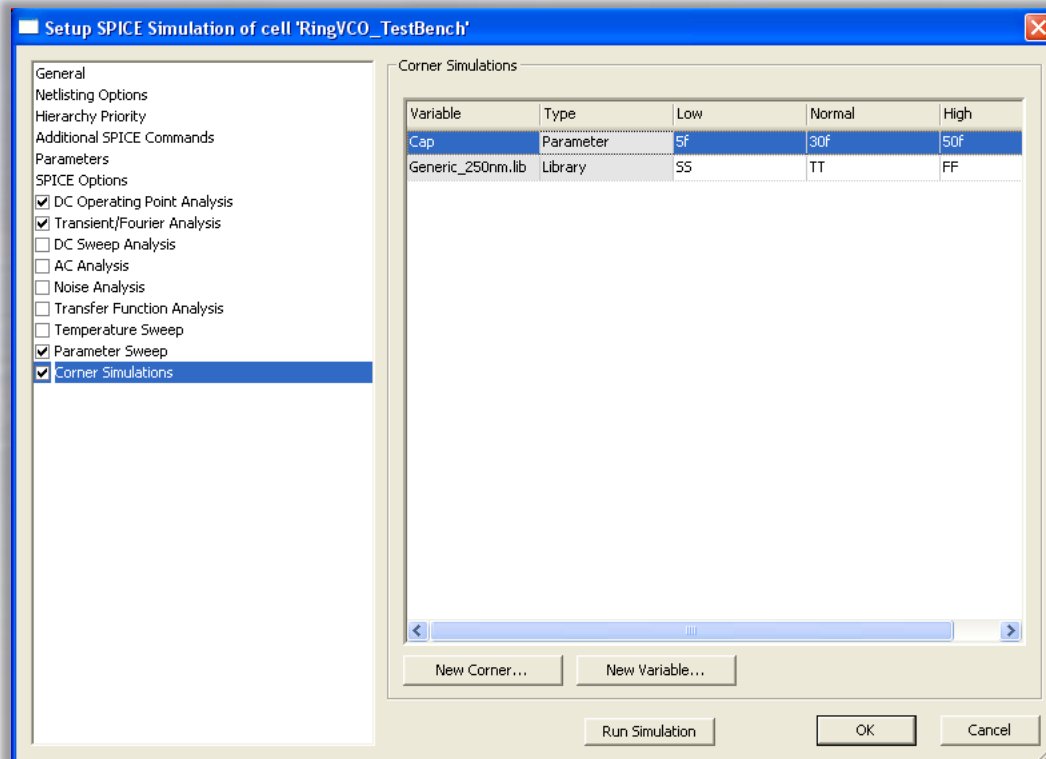
PMOS25
Control
DiffCell
RingWCO
C
V
Cello

```
Control:spice*
Imported from file C:\Documents and Settings\sbaswa\Desktop\temp\RingWCO_TestBench.sp

.subckt Control VTune Vb1 Vb2 Vbias Gnd Vdd
MM1p N_1 Vb1 Vdd Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u h=600
MM2p Vb1 Vb1 Vdd Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u h=600
MM3p N_2 Vb2 N_1 Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u h=600
MM4p Vb2 Vb2 Vb1 Vdd PMOS25 W=5u L=250n M=1 AS=3.25p PS=11.3u AD=3.25p PD=11.3u h=600
MM5n N_2 N_2 Vbias Gnd NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u h=600
MM6n Vb2 N_2 N_3 Gnd NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u h=600
MM7n N_3 VTune Gnd Gnd NMOS25 W=1.5u L=250n M=1 AS=975f PS=4.3u AD=975f PD=4.3u h=600
.ends
```

S-Edit: Additional Corner Simulation Settings

- Multiple .alter commands can now be inserted in a table format
 - Parameters, Temperature, Libraries, and TCL scripts can be added as variables
 - A desired value can be added as a corner
 - **File > Export > SPICE** has a check box to “Create separate files for each corner” so that consecutive results are not overwritten



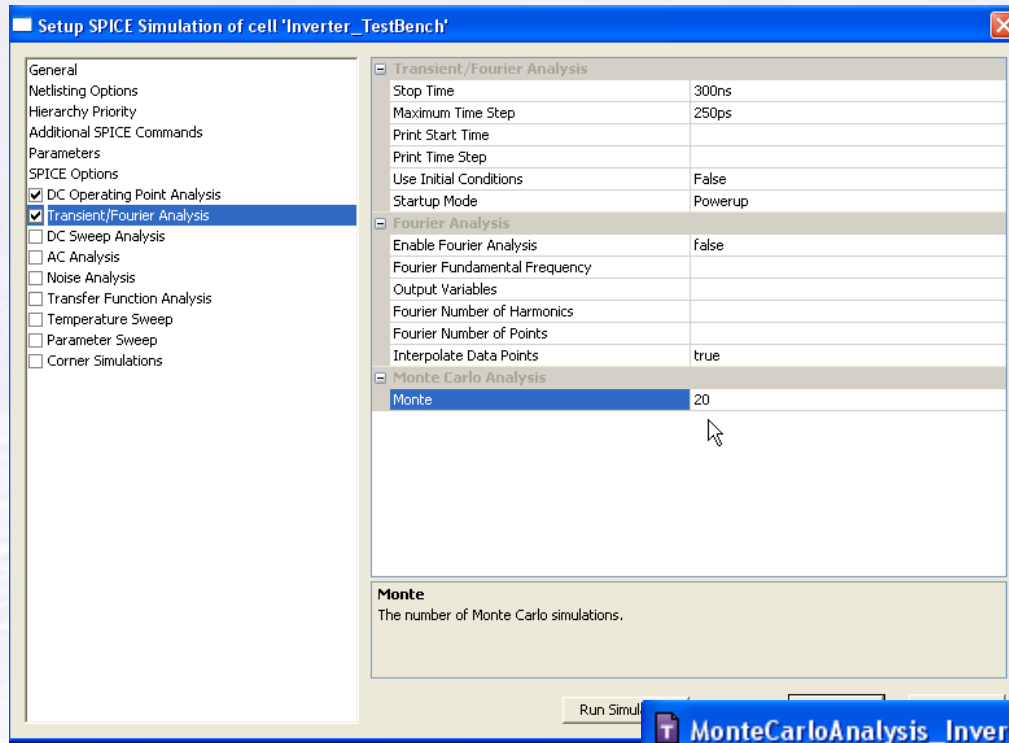
```
TransientAnalysis.sp *
***** Corners *****
.TITLE Low
.PARAM Cap=5f
.LIB "Generic_250nm_Tech/Generic_250nm.lib" SS

.ALTER Normal
.DEL LIB "Generic_250nm_Tech/Generic_250nm.lib" SS
.PARAM Cap=30f
.LIB "Generic_250nm_Tech/Generic_250nm.lib" TT

.ALTER High
.DEL LIB "Generic_250nm_Tech/Generic_250nm.lib" TT
.PARAM Cap=50f
.LIB "Generic_250nm_Tech/Generic_250nm.lib" FF
```

S-Edit: Monte Carlo Simulation Settings

- A Monte Carlo sweep option has been added to the applicable analysis options

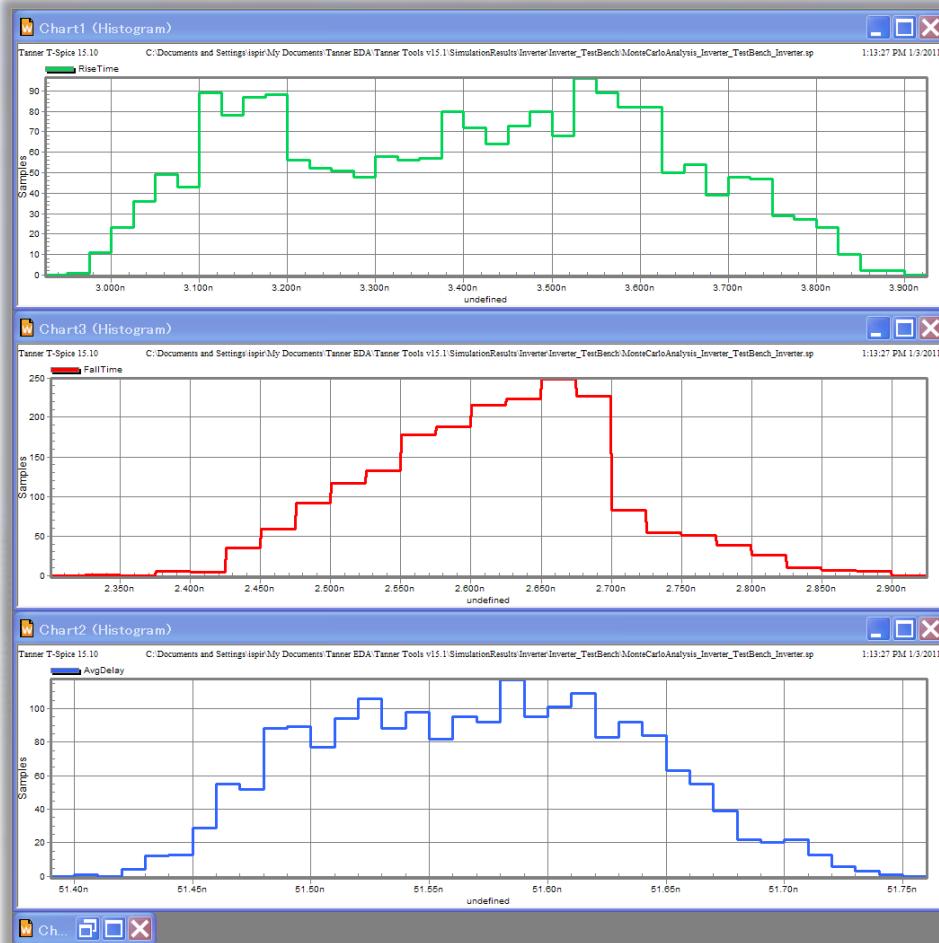


```
MonteCarloAnalysis_Inverter_TestBench_Inverter.sp

***** Simulation Settings - Analysis Section *****
.op
.tran/Powerup 250p 300n sweep monte=20
```

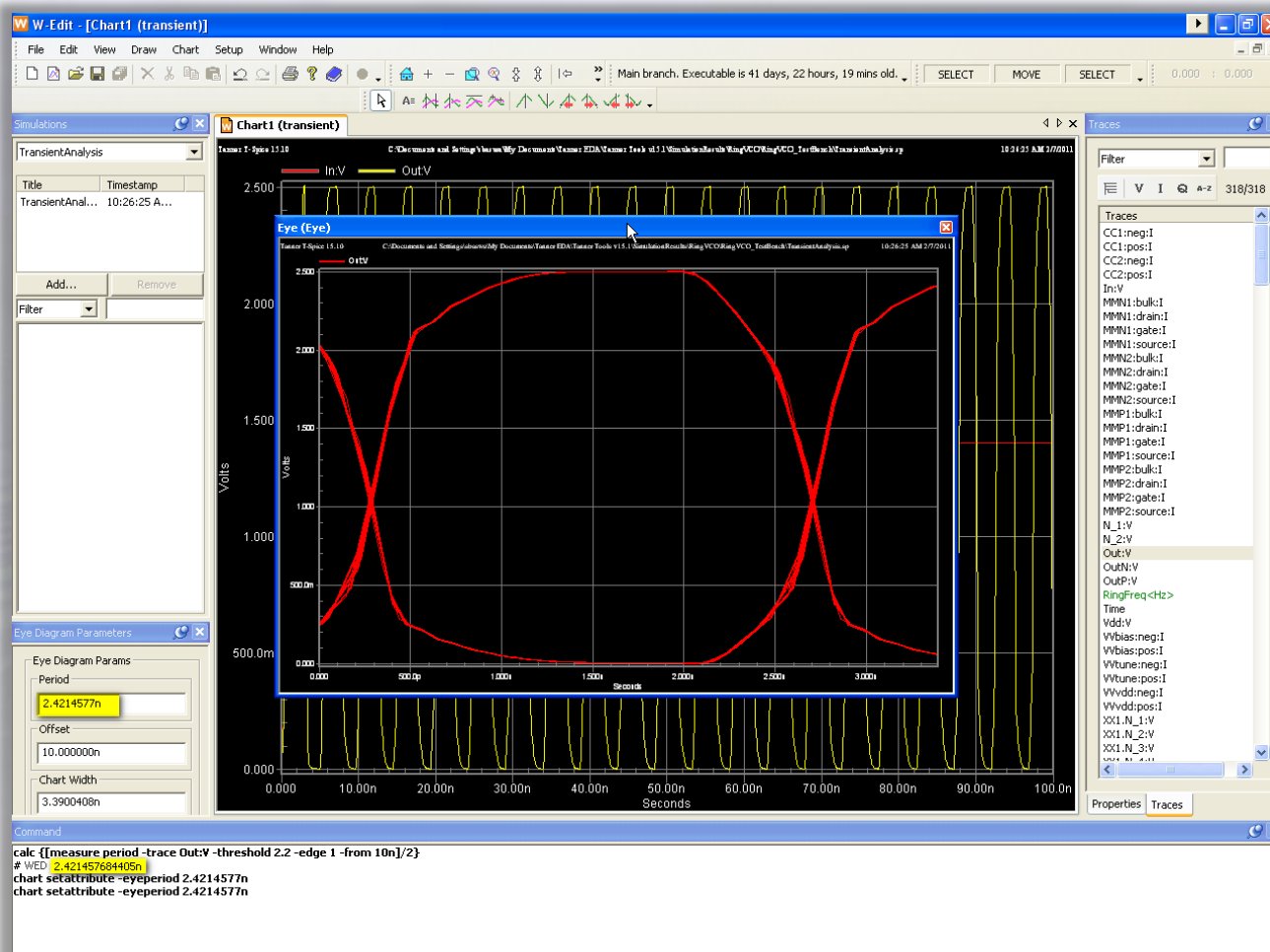
W-Edit: New Histogram Chart

- Results of .measure commands in Monte Carlo simulations are now automatically plotted on a histogram chart



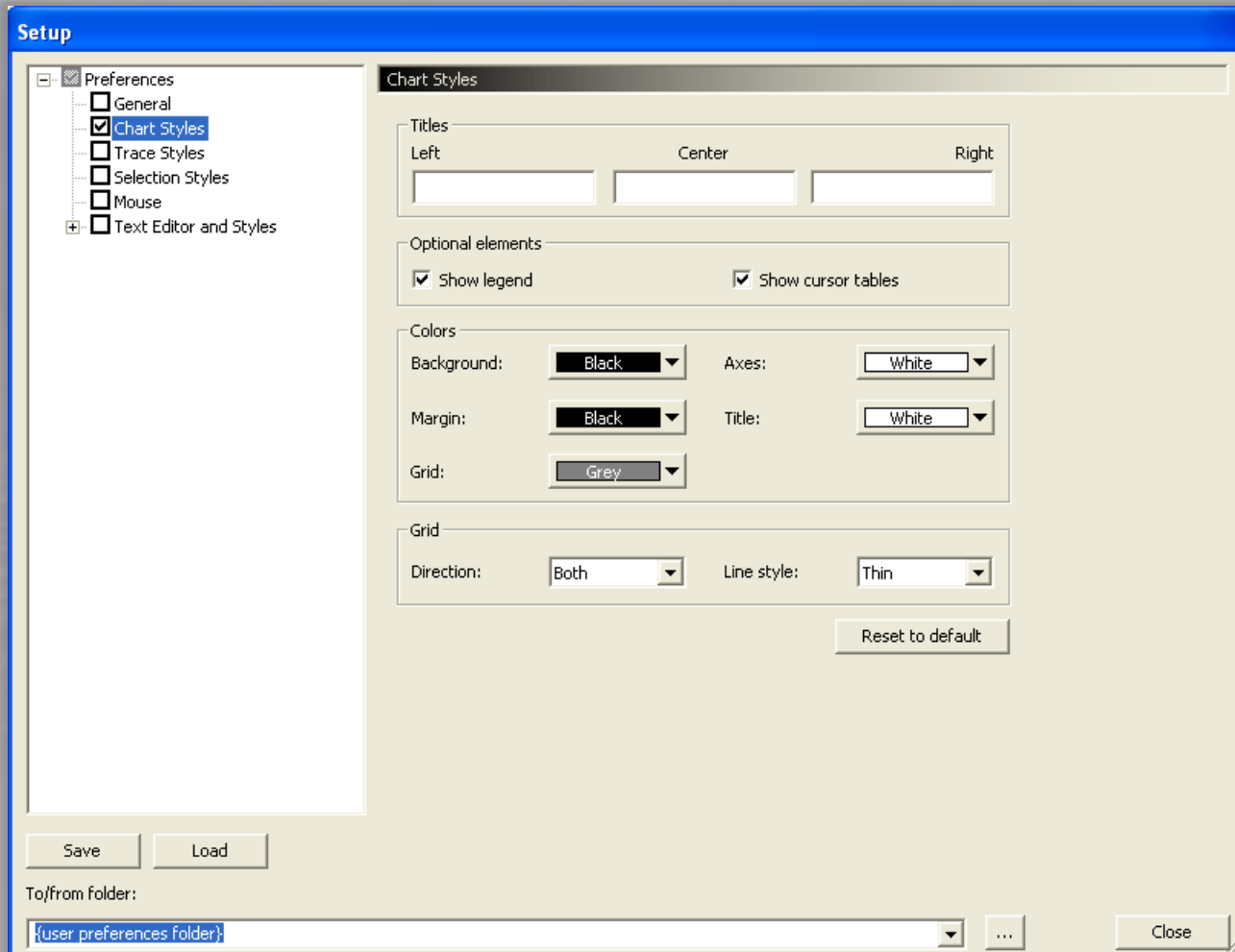
W-Edit: New Eye Diagram Chart

- Use **Chart > New Chart** to create a new Eye chart and then add a trace to the chart



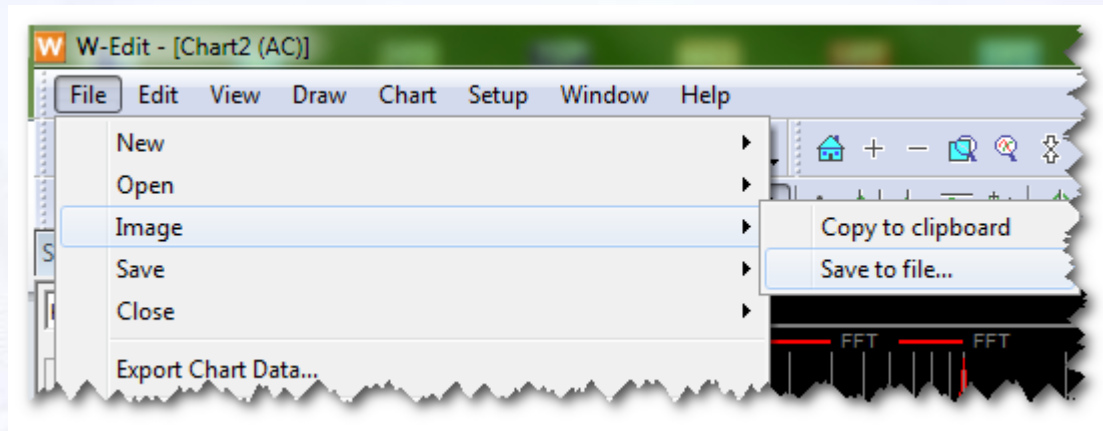
W-Edit: New Chart Style Setup

- Use **Setup > Chart Styles** to set global default display characteristics for charts



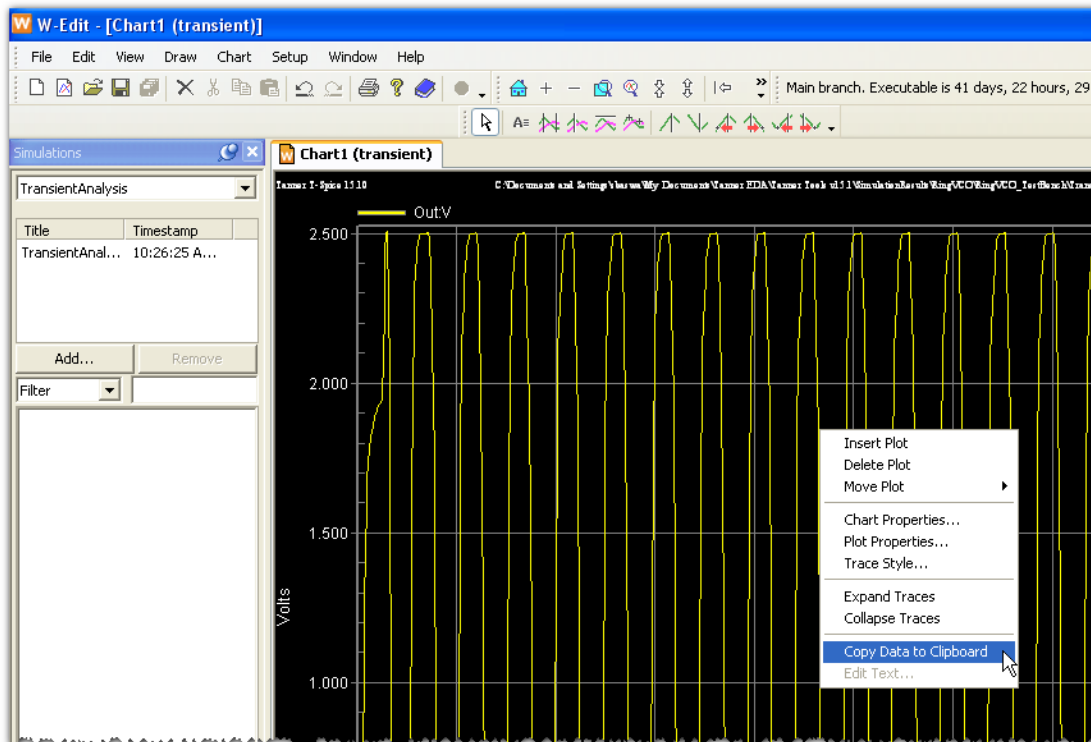
W-Edit: Copy or Save Charts as *.wmf

- **File > Image > Copy** to clipboard or **Save to file...** will save the image as a Windows MetaFile (.wmf)
- Windows MetaFile images can be then copied or imported to other applications.
 - Windows MetaFile is a Vector and Bitmap file format that enables high resolution display and printing



W-Edit: Import / Export Traces

- Traces can now be defined by reading data from a file or from the clipboard.
 - To define a trace from a file, use TCL command `trace define -file fileName -name traceName`
 - To define a trace from data in the clipboard, use TCL command `trace define -clipboard -name traceName`
- Chart data can now be copied to Windows Clipboard and pasted to Excel or any other external program
 - Right-click on the context menu of the selected trace and choose "Copy Data to Clipboard" command to copy the data to clipboard
 - When executed, it runs the TCL command `calc -clipboard`, which will operate when there is a singly-selected curve

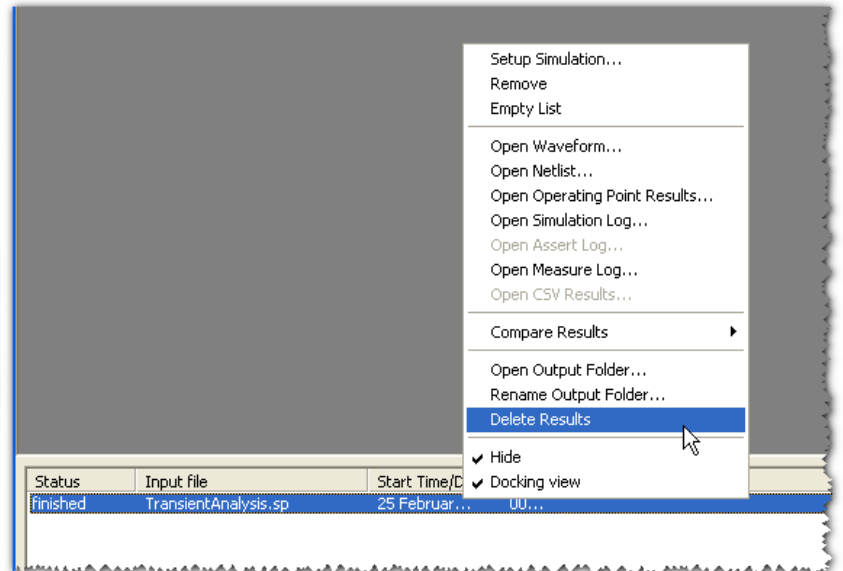
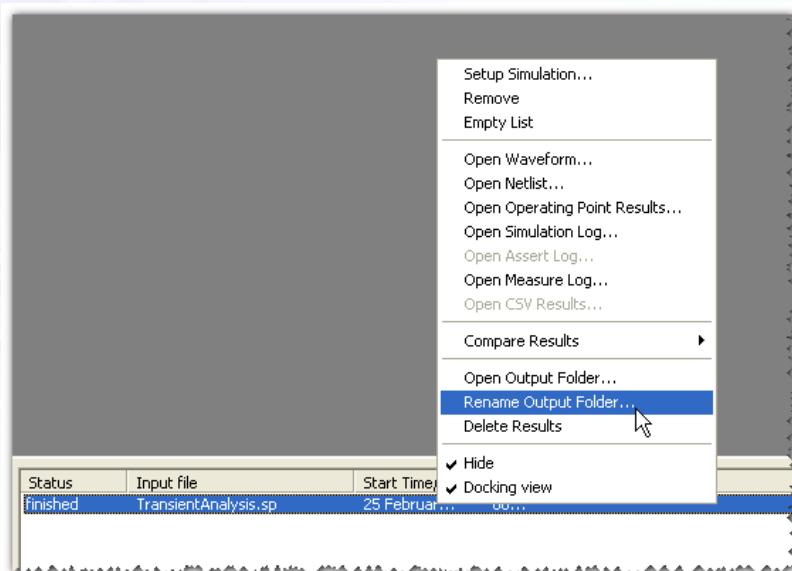


The screenshot shows an Excel spreadsheet with the following data:

	A	B	C	D	E
1	0	0			
2	6.25E-12	0.000126			
3	6.88E-11	0.015221			
4	2.69E-10	0.220043			
5	4.61E-10	0.580348			
6	5.58E-10	0.786875			
7	6.54E-10	1.00745			
8	7.63E-10	1.27323			
9	9.21E-10	1.59198			
10	1.00E-09	1.68042			
11	1.09E-09	1.734			
12	1.20E-09	1.77913			
13	1.35E-09	1.81967			
14	1.55E-09	1.85734			
15	1.75E-09	1.8866			
16	1.95E-09	1.91029			
17	2.15E-09	1.9275			
18	2.35E-09	1.9357			
19	2.55E-09	1.9422			
20	2.74E-09	2.23401			

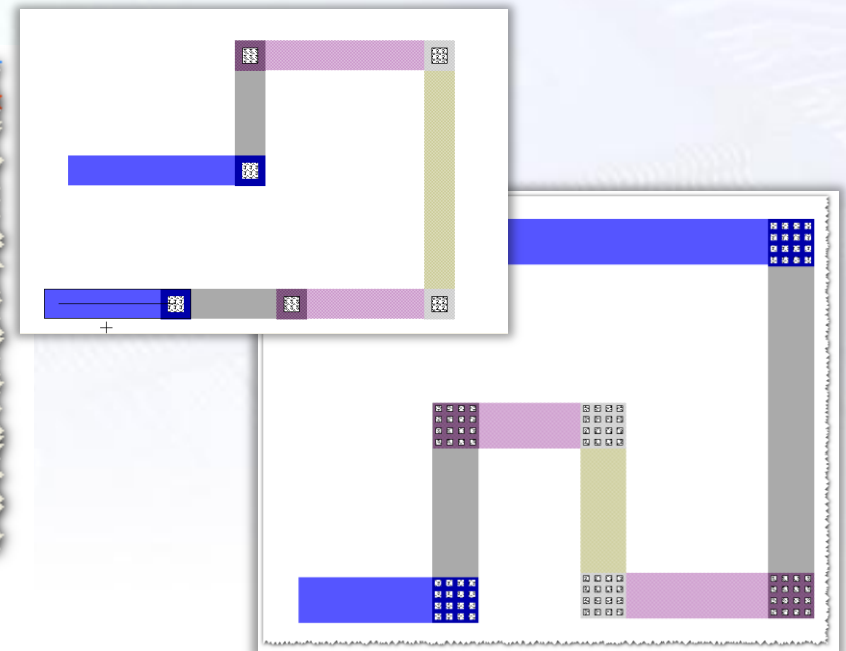
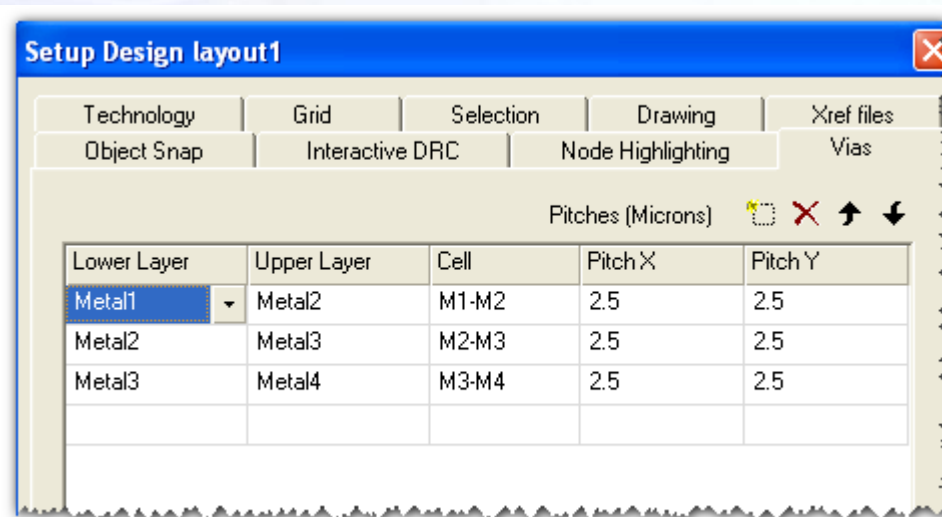
T-Spice: Simulation Files/Folders Can Now be Easily Renamed

- From the Simulation Manager, Right-Click the simulation and select **Rename Output Folder...**
 - Command was previously used to rename the database output folder
- **Delete Results** deletes the results database and .tsim simulation command file simultaneously



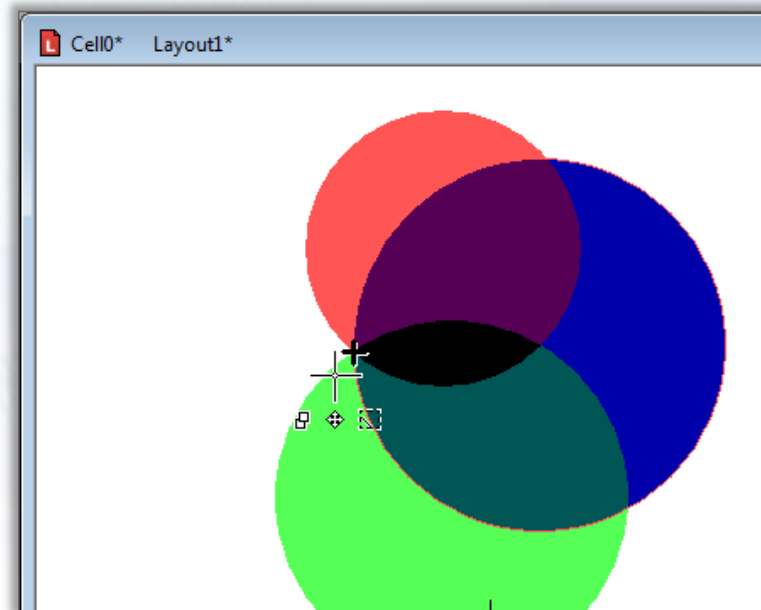
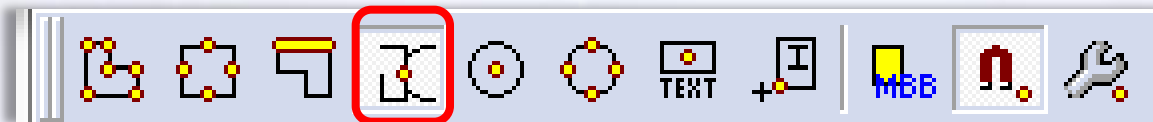
L-Edit: Improved Wire Drawing with Vias

- Manual routing is much faster with improved Via placement tools
 - While drawing a wire, press the hot key to place a contact/via
 - Draw > Contacts > Down** Key “[” or **Draw > Contacts > Up** Key “]”
 - The command will now end the wire, place a contact/via, and start a new wire, all with one key stroke
- A Vias tab has been added to the **Setup > Design** dialog which allows for the setup of contact/via cell connection layers and spacing
 - The tab settings are used by **Draw > Contacts > Down** Key “[” or **Draw > Contacts > Up** Key “]” while drawing wires.
 - Contacts created with **Draw > Contacts > Define Contacts** or **Guarding** are automatically added to this tab



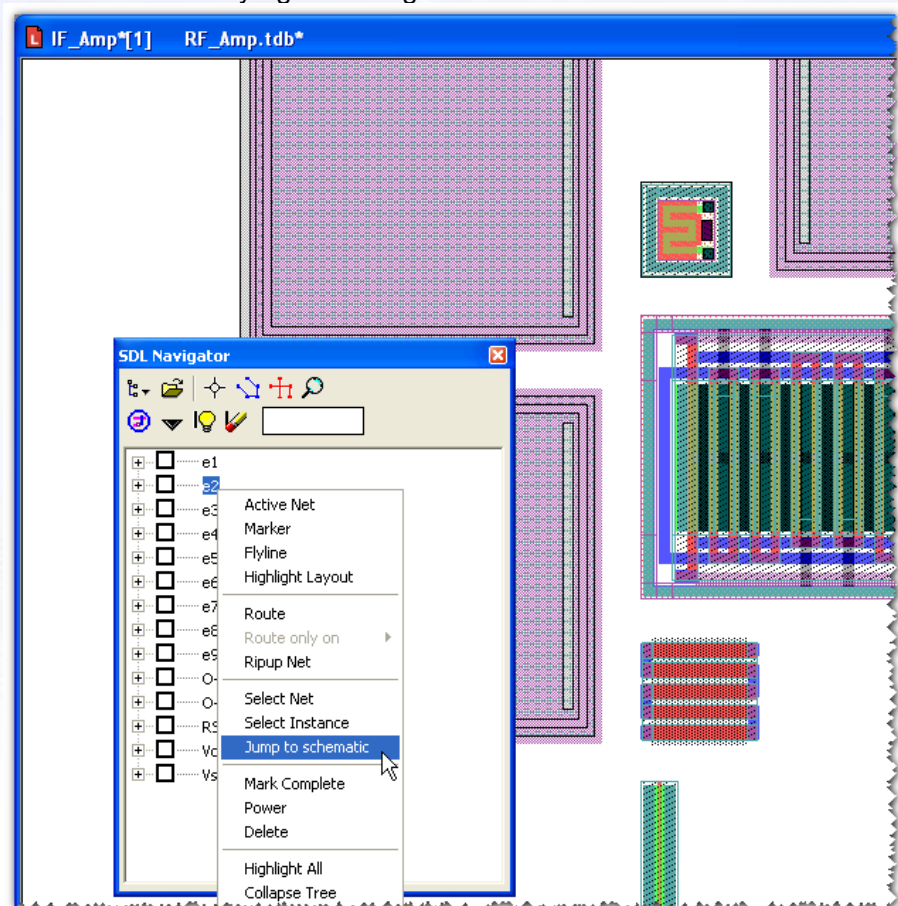
L-Edit: Snap to Intersection

- A new object snapping mode is available allowing you to snap to intersections
- Snap to Intersection operates on all objects (boxes, polygons, wires, circles) and works through hierarchy



L-Edit: SDL Jump to Schematic

- When a net or instance is selected in the SDL Navigator in L-Edit, you can now highlight that net or instance in S-Edit
 - Use the SDL context Sensitive menu by right-clicking



HiPer Verify: DRC / Extract Speed Improvement

- The performance of HiPer Verify extraction is significantly improved for certain designs which utilize an EXTENT calculation
 - Several designs were extracted close to four times faster
- The BEVEL option in the Calibre SIZE command is now supported

HiPer DevGen: Added Resistor Arrays

- The resistor generator in HiPer DevGen now has the ability to create resistor arrays
- SDL recognizes resistors in a netlist that have the same L and W and combines them into one resistor array

