

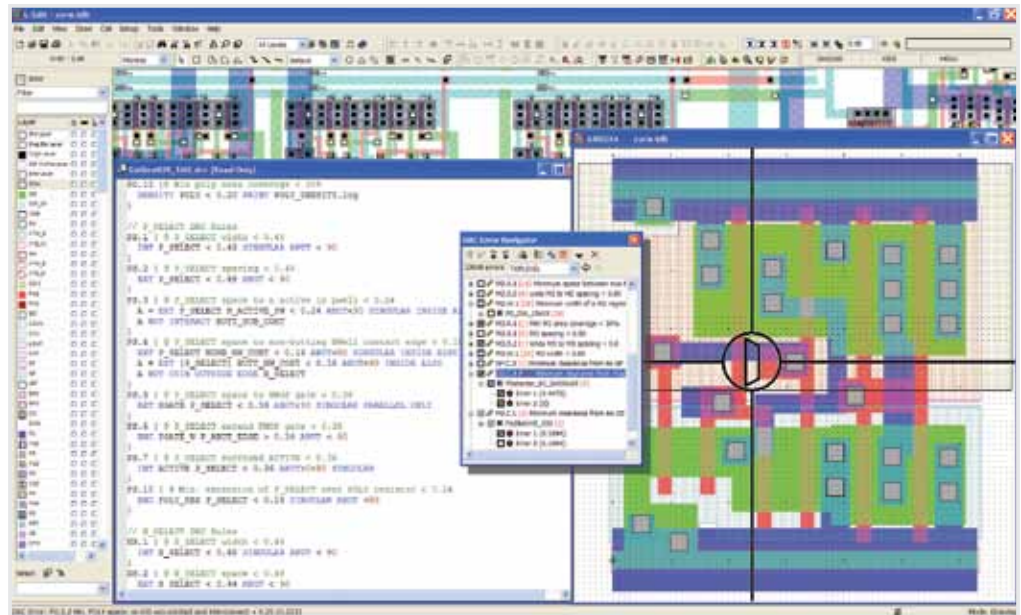
HIPER VERIFY FOR VERIFICATION

Product Benefits

- Speeds verification and increases productivity.
- Delivers performance and functionality at a fraction of the cost.
- Enables faster and simpler debugging through hierarchical DRC and netlist extraction.
- Meets the most challenging submicron verification requirements.
- Supports a broad range of technologies for analog, mixed-signal, and MEMS applications.

Product Features

- Integrates with L-Edit™ layout editor for precise location of violations.
- Runs Calibre®, Assura® and Dracula® foundry files natively, without conversion or modification.
- Performs background processing to allow you to fix violations while DRC is still running.
- Delivers enhanced layer generation and advanced rule file editing.
- Supports orthogonal, 45°, all-angle and curved layouts.
- Performs electrical rule checks (ERC) such as antenna checks.
- Provides density checking commands with stepping and overlapping windows and multi-layer expression options.
- 64-bit engine for increased capacity and higher performance.
- Display short and open circuit warnings in the layout.
- Extract a hierarchical SPICE netlist from layout for LVS and post-layout simulation.
- Provides default property computations for built-in devices or user code may be written to compute custom properties from a set of pin and auxiliary layers.
- User-defined devices (subcircuits) can be specified for extraction of functional blocks or unusual devices.



Speeding Concept to Silicon

When you're performing physical verification of your analog and mixed-signal IC designs, speed is the name of the game. You need tools that support you in speeding products to market. These tools must also deliver a level of accuracy that ensures correct-by-design and error-free layouts. They must be compatible with your foundry, eliminating the need for time-consuming conversion or modification of command files.

Tanner EDA's HiPer Verify™ is a comprehensive yet affordable solution for analog/mixed signal IC design rule checking (DRC) and netlist extraction on the Windows® or Linux® platform. HiPer Verify uses advanced hierarchical algorithmic techniques to provide optimal performance for your designs.

Easily maintain foundry compatibility

Most foundries provide DRC and LVS rules in Calibre, Assura or Dracula format. When you change your process or feature size, you must update your DRC & LVS rules—a time-consuming process.

HiPer Verify can run Calibre, Assura and Dracula rule files directly from the foundry. When your verification process changes, you can simply reference the new DRC or LVS command file from the foundry, meeting your existing standards right out of the box. You get the security of knowing you are running your rule files without modification or conversion, and the convenience of not having to perform translations.

- Execute multiple DRC command files sequentially in a single DRC run.
- Run batch DRC or netlist extraction on multiple cells.
- Perform powerfully complex checks required for 130nm and below.
- Verify your most complex analog or mixed-signal designs through support for orthogonal, 45°, all-angle, and curved layouts.
- Run a single DRC rule directly from the command file.

- Perform electrical rule checks (ERC) in addition to design rule checks (DRC), through support for connectivity-based DRC rules including antenna checks.
- Extract a hierarchical SPICE netlist from layout using a Calibre or Dracula format LVS command file.
- Perform default property computations for built-in devices or create user code to compute custom properties from a set of pin and auxiliary layers.
- 64-bit engine provides increased capacity and higher performance which is critical when designing today's complex designs.

Increase productivity with hierarchical DRC and netlist extraction

HiPer Verify's verification engine is designed to take advantage of the hierarchy and repetition in today's IC designs. This engine provides significant performance improvements over flat verification engines and makes it much simpler to interpret the results. HiPer Verify's hierarchical rule checking engine finds violations in the cell where they occur. This enables you to correct a violation once rather than sorting through many duplicate violations as flat processing requires.

- HiPer Verify's hierarchical extraction engine generates a hierarchical netlist for easier LVS. With its ability to extract advanced device parameters or parasitics, you will be able to perform more accurate post-layout simulations.
- Integrated with Tanner EDA's L-Edit™, making it quick and easy to run DRC and to view and fix DRC violations.
- Run DRC in the background so you can continue layout or fix DRC violations while DRC is still running.

Find and fix violations quickly

In a typical verification cycle, you will spend more time fixing violations than running the verification tool. HiPer Verify speeds the process with an advanced Verification Error Navigator that takes you instantly to the location of a violation in the layout editor and provides a clear and thorough summary report of DRC and extraction results.. It opens the cell and centers the layout exactly on the selected violation, making it easy to see and correct.

- View violations in either the top cell or the cell where the violation occurred.
- View the required rule distance and the actual violation distance.
- Mark violations as they are fixed so you can save your progress. When you open the design again, you will know which errors still need to be fixed.
- Zip through LVS with cross-probing between schematic, layout, SPICE netlists and LVS results to highlighting nets or devices and with enhanced navigation of SPICE files.
- Import DRC results from a Calibre DRC results file for viewing in L-Edit.

Edit DRC and LVS command files easily

Composing and debugging command files requires specialized knowledge of command language syntax. HiPer Verify includes a text editor specifically designed for speeding up the job of editing DRC and LVS command files. HiPer Verify's rule editing environment has syntax (keyword) highlighting to assist in rule file creation.

- Right-click on a layer name in the rule file to view the full layer derivation tree or instantly generate the layer in the layout editor.

Reduce verification costs

Increase your number of verification licenses without increasing your overall tool costs. With its native compatibility, you can integrate HiPer Verify into your existing tool flow with little effort. By purchasing fewer expensive tool licenses and using them only for final verification, you will save money and reduce your maintenance costs.

Benefit from flexible licensing

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. HiPer Verify is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, HiPer Verify will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, HiPer Verify does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

"Tanner Tools have helped make us a winning team. We initially chose Tanner Tools to minimize costs. But we soon discovered that the T-Cell, Schematic Driven Layout, and verification capabilities of the tools help improve our design efficiency and shorten our design turnaround time. Using T-Cell, we've shortened our block layout design by 60%. Plus, L-Edit can load Calibre DRC result files, which makes it very easy to find and fix errors. We plan to make our design procedure more effective using Tanner's HiPer Verify."

—Miyoko Goto
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Find out what HiPer Verify can do for your design challenges.
Contact us at DesignChallenge@tannereda.com for a 30-day evaluation.

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