

Tanner EDA Today

Driving Analog Innovation



From the President: Productivity and the Full-Flow Analog IC Design Suite



What's New in Tanner Tools: v15.1



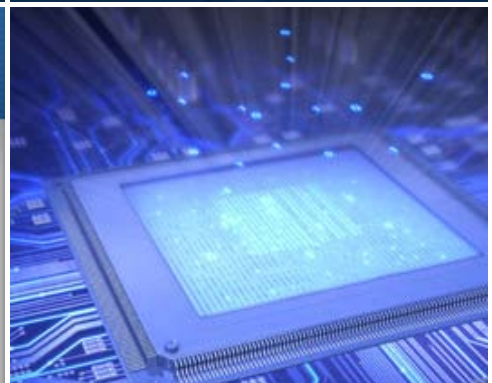
**FAE Focus:
Jie Meng, Senior Application Engineer**



**Analog Insights:
What is the Hype About HiPer Verify?**



**Partner Spotlight:
Singapore – Advinno Technologies**



**Tips & Tricks:
From Jie Meng**

From the President: Productivity and the Full-Flow Analog IC Design Suite



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The need for productivity and efficiency in today's analog IC marketplace is increasingly apparent. With pressures to reduce cost with greater resource constraints, organizations need to consider ways in which they can eliminate extra or unnecessary steps and redundancies in their analog IC design process. The most useful improvements, aside from ensuring fewer errors and delays, will help them get to market faster with minimal touch points.

In my professional life, I spent many years in the world of ERP where the idea of a single integrated solution prevails and the value add exists in bridging the intersections of organizational functions and processes uninterruptedly – for a seamless flow, if you will. In addition, with one integrated solution, there is one go-to provider for service and support that understands how a myriad of moving parts are working (or not working) together. Because this software/ systems provider can deliver bigger picture results and solutions to challenges throughout the flow, this provider becomes a more invested partner, with insight into all aspects of an enterprise and how they inter-connect.

“ I personally believe in the philosophy behind Tanner EDA's full-flow analog IC design suite and in the value it brings to customers. ”

It is therefore from the direct experience of seeing the longer-term ROI from time, labor, and cost savings achieved through seamless integration that I personally believe in the philosophy behind Tanner EDA's full-flow analog IC design suite and in the value it brings to customers. Tanner's full-flow design suite is an integrated front-end to back-end product package that shares a common architecture and common user interface that is consistent across all tools. This uniformity results in a comprehensive, cohesive software solution that maximizes design productivity while simultaneously reducing total cost of ownership.

Often we will “spotlight” certain individual products or point tools to highlight specific features and benefits on our Web site, in our datasheets, or webinars and we have and will continue to do so in this newsletter. And although we sell many of those tools on their own and have numerous customers using our standalone tools successfully—such as in the area of back-end layout with L-Edit—for those designers who touch all stages of the analog IC design cycle, front-end to back-end, Tanner EDA's full-flow tool suite can offer substantial advantages.

I invite you to take a closer look at our full-flow tool suite via our [video demonstration](#) and / or to [try it for free](#) through evaluation.

- Greg Lebsack, President

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Analog Insights: What is the Hype About HiPer Verify?

Many of users have experienced the benefits of Tanner EDA's verification tool as part of their full-flow design suite. What customers should know is how they can reduce their workload and get even better results with our enhanced physical verification tool, HiPer Verify.

[Technologies](#)

[Happenings @ Tanner](#)

Happenings @ Tanner

Tanner EDA Will Be Participating in the Following Upcoming Industry Events:

[DesignCon 2011](#) Jan 31 - Feb 3

Tanner EDA will be presenting "[Breaking through the Analog IC Layout Design Bottleneck](#)" and will host a panel: "[PDKs for Analog IC Design--A Stakeholder Discussion](#)".

[EDS Fair 2011](#) Jan 27 & 28

in Kanagawa, Japan

[Date 2011](#) Mar 14 - 18

in Grenoble, France

[Learn more about Tanner EDA events](#)

Participate in our Webinars

HiPer DevGen:

December 14 – 2:00-3:00 pm PDT

December 16 – 8:00-9:00 am PDT

HiPer Verify:

January 11 – 2:00-3:00 pm PDT

January 13 – 8:00-9:00 am PDT

L-Edit:

January 18 – 9:00-10:00 am PDT

January 20 – 2:00-3:00 pm PDT

Check out our [Webinars homepage](#) for more topics, dates, and times because we are always adding new sessions!

[Sign up for training at Tanner in Monrovia, CA](#)

What's New in Tanner Tools: v15.1

Tanner's full-flow suite is now better than ever with the release of v15.1 of our tools. See for yourself how Tanner EDA is driving analog innovation.

L-Edit Improvements

- Wire drawing productivity enhancements

With HiPer Verify, companies can eliminate the need for costly sign-off tools entirely or supplement the use of short-term licenses for sign-off tools with iterative verification throughout the design process to catch and correct errors early on. This can reduce the unpredictable cost, workload, and resulting stress at the close of a tape-out deadline.

What makes HiPer Verify distinct from standard verification and allows it to work alongside sign-off tools throughout the design process or also perform as the sign-off tool on its own is its use of foundry compatible hierarchical DRC and its ability to run a foundry rule file without conversion.

Design Rule Checking (DRC)

In addition to the rules checked by Standard DRC, HiPer Verify can check antenna rules, connectivity-based rules, and rules requiring complex geometric functions. Because HiPer Verify can check the whole sign-off deck, there are fewer chances of surprises at tape-out when running the sign-off tool.

HiPer Verify runs Calibre®, Assura®, or Dracula® DRC rule files from the foundry, without conversion. Design engineers therefore have the security of knowing they are running rule files without modification with the convenience of not having to perform translations. This saves enormously on time spent setting up and testing rules manually.

Additionally, switching to a new rule deck is easy with HiPer Verify, whether it's an update of an existing process or the switch to a whole new process. The user simply has to refer the new command file from the foundry, and they are ready to go!

Extract

HiPer Verify can run Calibre® and Dracula® LVS rule files directly from the foundry.

HiPer Verify supports specialty processes, such as for high voltage, and advanced process nodes. The tool enables extraction of complex devices (i.e. LDMOS) and advanced device parameters (i.e. LOD / STI, WPE, etc.). Precise post-layout simulation on advanced process nodes requires such parameters.

HiPer Verify is fully a hierarchical layout extractor, and can export a hierarchical netlist from the layout. Hierarchical extracted netlists make LVS debugging easier.

See for Yourself What a Difference HiPer Verify Makes

If you are currently using Tanner tools and standard verification and would like to try HiPer Verify, please sign up for a free evaluation and see for yourself what the hype about HiPer Verify is all about.

[Request an Eval of HiPer Verify](#)

[Visit our Web site to learn more about HiPer Verify Physical Verification](#)

[Download the HiPer Verify Datasheet](#)

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- Modifications to Router Setup

[L-Edit Datasheet](#)

S-Edit Enhancements

- Improved connectivity views
- Enhanced access control of designs allows easier team collaboration
- Corner simulation setup

[S-Edit Datasheet](#)

T-Spice

- Improved transient simulation performance (DC convergence) with documented 20% improvement due to new compiler and solver
- Update of Verilog-A, SimKit, and BSIM4 SOI models

[T-Spice Datasheet](#)

HiPer Verify Enhancements

- Extent optimizations
- Support for size - bevel option

[HiPer Verify Datasheet](#)

W-Edit

- Histograms
- Eye diagrams
- Performance improvements

[Learn more about W-Edit](#)

HiPer DevGen Layout Acceleration

- Resistor arrays

[Learn more about the HiPer DevGen tool offering](#) and view our video demonstration

Partner Spotlight: Singapore - Advinno Technologies



In May of 2010, Tanner EDA appointed Advinno Technologies of Singapore to provide regional representation in Southeast Asia.

F&E Focus: Jie Meng, Senior Application Engineer



Jie Meng is a Senior Applications Engineer at Tanner EDA's headquarters in Monrovia, California. He grew up in middle China and received his Bachelors degree in Electrical Engineering. Jie later went on to complete his M.S. in Electrical Engineering in the United States. He joined Tanner EDA in 2004 and is currently focused predominantly on PDK development work.

In his free time, Jie enjoys meditation, hiking, ping pong, and surfing the Internet. He attributes his ability to avoid getting sick to his meditation practice.

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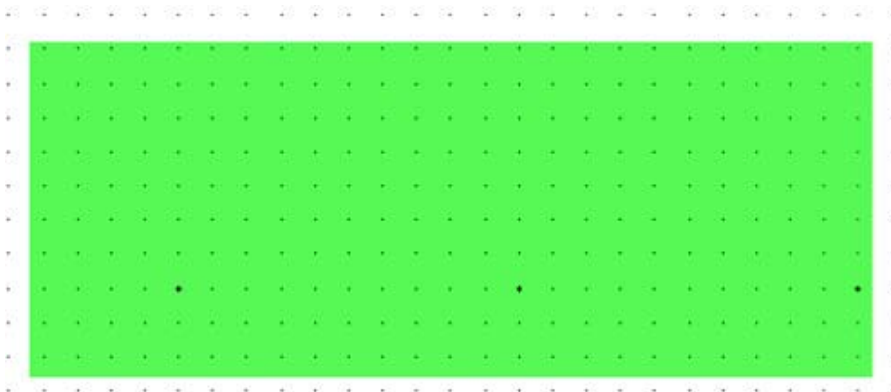
Tips & Tricks


From Jie Meng, Senior Application Engineer and this quarter's F&E Focus:

Tip #1: Boolean / Grow Operations

One feature I would like to share is the Boolean/Grow operation, which allows users to create new patterns based on existing patterns.

As an example, say I plan to draw an N Select layer over an Active layer that surrounds the Active by a specified distance. To do this easier, can draw the Active layer first as shown below.



Next, I select it, and then press hotkey B. Alternately, I can select the Boolean/Grow Operations icon  or go to Draw > Boolean / Grow Operations a dialog box will appear as follows:

Advinno provides sales and support for all Tanner EDA products in Singapore, Malaysia, Thailand, Vietnam and Indonesia. Terry Teh, President and Co-Founder of Advinno joined us for a brief Q&A for this quarter's issue of Tanner Today:

Q: Please tell us about Advinno Technologies.

A: Advinno is a privately-held design solution company incorporated in Singapore and with offices in China, Malaysia, and Vietnam. Our goal is to provide customers with best-in-class solutions such as EDA, IP, FPGA and ASIC, and embedded as well as design services, training, and consultation.

Q: What made Tanner EDA and Advinno a good fit for partnership?

A: Our focus is on enabling customers to deliver first-pass design success within the shortest possible time to market by using best-in-class design solution. Tanner has been helping designers reach those same goals for two decades now. We are very pleased to be able to add this top quality line of products to the set of solutions we can offer our customers.

Q: Does Advinno offer all of Tanner EDA's tools to the Southeast Asian market?

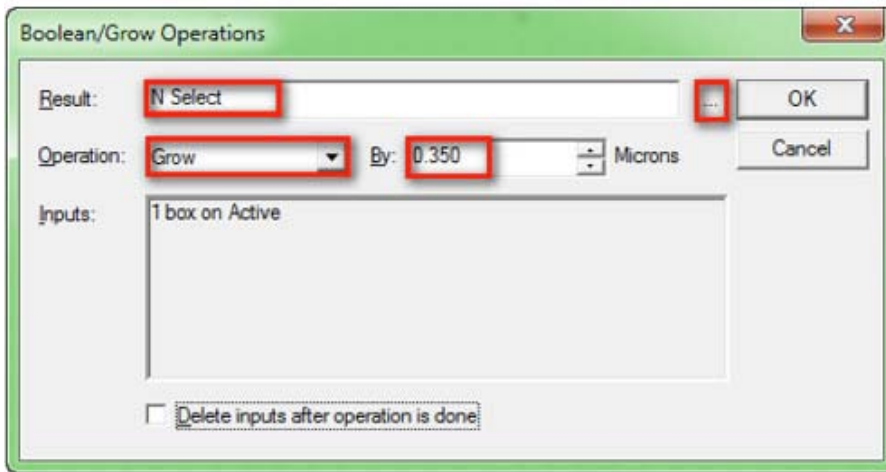
A: Yes - we cover sales of Tanner's full-flow analog IC design suite, HiPer Silicon, as well as related specialty design tools and services.

Q: Which is the biggest market segment served by Advinno? Is it commercial or educational? What design types?

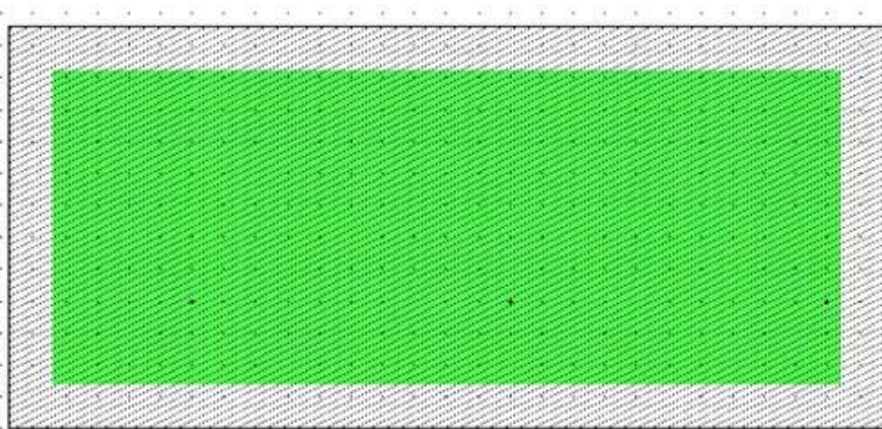
A: Our customers for Tanner tools fall within academic, commercial and research institutions. While they are really developing applications across industries, it is fair to say our users are heavy in analog IC design, MEMS, and power management.

Q: What are some of Advinno's plans or goals in the near future regarding the sale and support of Tanner tools in the region?

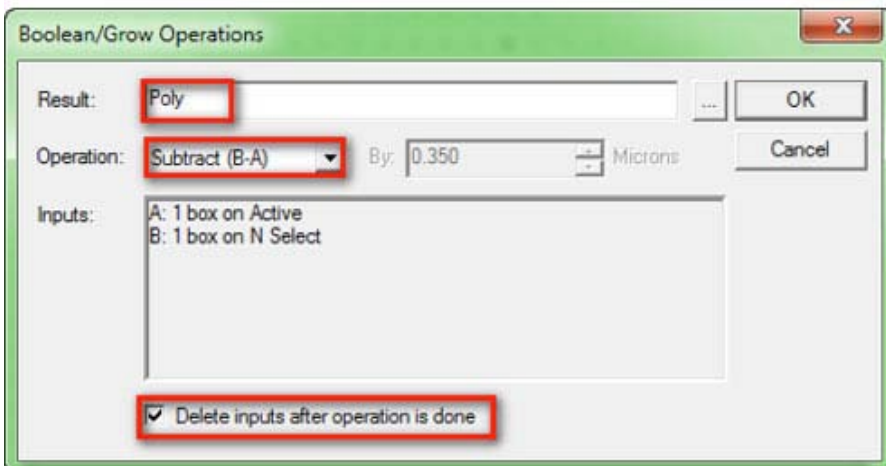
A: At this point our focus has been government and research centers in Singapore and Malaysia.



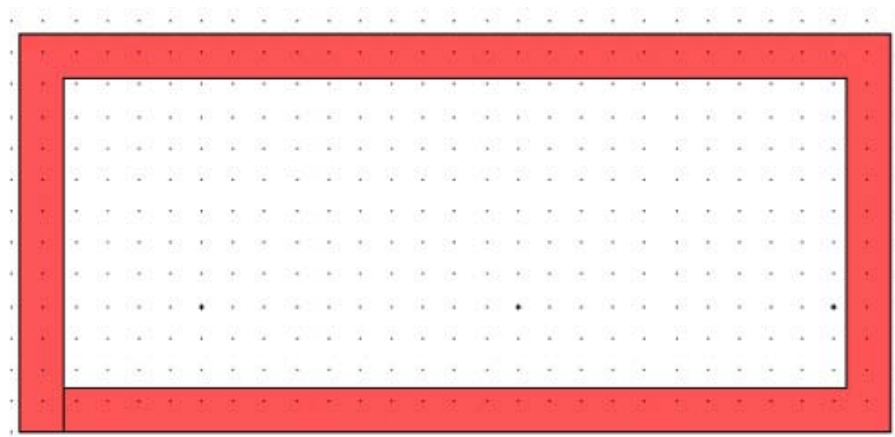
I can choose the resulting layer by pressing on the ... icon and selecting the N Select layer. I can then select the Grow operation, which will grow all edges of the selected polygon (our Active region) by the specified amount. Set the grow amount to a value that follows the DRC rules for your process and then select the OK button. This will generate the following pattern:



Now, say I want to create a structure on Poly that is the shape of the N Select ring around the Active region. I can also do this quickly using Boolean/Grow Operations. Just select the above two boxes and again press the B hotkey. Choose the result to be on Poly and choose the Subtract (B-A) option such that you will be subtracting A: 1 box on Active from B: 1 box on N Select. Make sure you also check the box that reads "Delete inputs after operation is done".



This will create a ring structure as shown below:

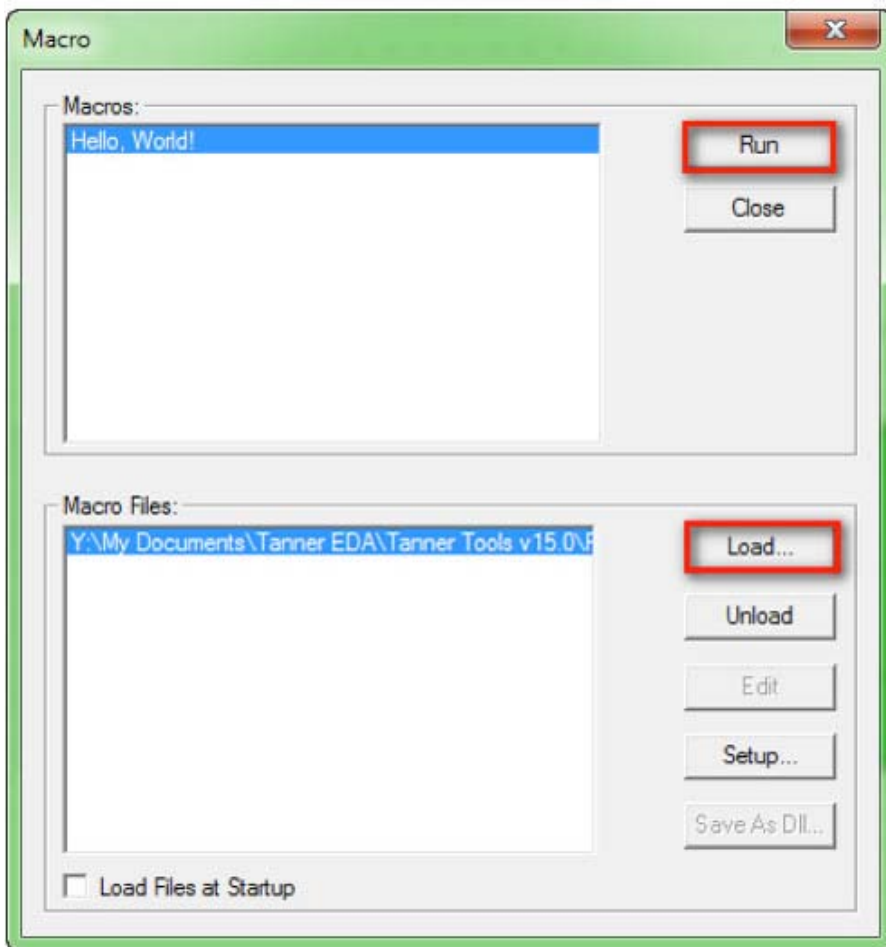


Tip #2: Save UPI Macro to DLL (Dynamic Link Library)

Sometimes users do not want to share their UPI macro source code with everyone that will be using the macro. With this tip, macro writers can save their UPI macro to a compiled DLL directly from L-Edit and thus only share the DLL with others and not the source code.

In L-Edit, open the UPI macro source code by dragging and dropping the .cpp or .c file into L-Edit or by selecting File > Open and browsing to the UPI Macro file. Once open, select Tools > Save as DLL. This will save the source code to a DLL file.

To load the DLL, just select Tools > Macro and the dialog will appear as follows:



Click the Load button to load in the DLL, then highlight the function (here it is Hello, World!), then click the Run button to run the macro.

You can also select the option Load Files at Startup, which will allow the macro to be automatically loaded when L-Edit starts.

If a .c or .cpp macro is loaded into this Macro dialog, you can also select it and press the Save as DLL... option directly from this dialog. You would then just need to unload the .c or .cpp macro and load or distribute the .dll compiled macro.

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