

# Tanner Tools v14.13

## Release Notes

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# Tanner Tools Version 14.13

## What's New in S-Edit v14.13

- There are no new features in S-Edit v14.13.

## What's New in T-Spice v14.13

- Fixed a crash in T-Spice due to expression controlled devices issuing warning messages during multi-threaded simulations.
- Fixed fatal error when probing currents of Verilog-A devices.
- Fixed problem where expression controlled devices could cause a crash in certain circumstances.

## What's New in W-Edit v14.13

- There are no new features in W-Edit v14.13.

## What's New in L-Edit Pro v14.13

- Fixed problem in GDS export. When “Restrict cell names to 32 characters (or 128 characters)” is set, cell names would be truncated and a warning would be issued, but the resulting GDS file could have duplicate cells with the same name as a result of the truncation. Cells are now renamed uniquely after truncation.

## What's New in HiPer Verify v14.13

- There are no new features in HiPer Verify v14.13.

# Tanner Tools Version 14.12

## What's New in S-Edit v14.12

- "Zoom to Selection" has been improved to (1) zoom in so that selection occupies no more than 1/2 the screen (used to be 1/3 the screen), and (2) never zoom out further than the "home" view.
- When importing Cadence EDIF, for non-primitive cells, the SPICE.OUTPUT property now contains  $\${Cell}$  at the end. This is used to place the subckt name in the Spice netlist.
- Fixed crash running a script when opening a design with docked graphical views.
- Verilog export now obeys VERILOG.PRIMITIVE = true.
- Views with Unicode view names are now saved and opened correctly.
- Improvements are made to netlabel snapping performed on importing EDIF.
- Fixed quotation problems when exporting library paths to the Spice netlist.
- Under Setup Spice Simulation > General > Accuracy and Performance, added the Precise option.
- S-Edit now exports the expression 'a ? b : c' correctly.
- Problem where not all views of a cell were being exported is fixed.
- Fixed problem in exported Spice node names when symbol ports names contain "\_".
- Problems redirecting instances are fixed.
- Fixed problem when exporting spice in the case where a net is connected to a port that has a different name.

## What's New in T-Spice v14.12

- Fixed problem where T-Spice would crash if a subcircuit instance has more node connections than the original subcircuit definition requires.
- Fixed problem where T-Spice would fail when the input file contains string .param values, for example param matchingGroup=str("NONE").
- Fixed problem where using the .ic command within a subcircuit definition to assign the current through an inductor would cause T-Spice to fail.
- BJT And VBIC now correctly test for Vbc and Vbe values relative to  $VT * KT/Q$  to determine the operating region.
- Made corrections to the printed transistor terminal currents when the device M multiplier term is set.
- Fixed problems with some 64 bit Verilog-A transient simulations that were not running to completion.

## What's New in W-Edit v14.12

- There are no new features in W-Edit v14.12.

## What's New in L-Edit Pro v14.12

- LVS no longer crashes when .OPTION parhier is set to local.
- Node Highlighting by name now works correctly when a port overlaps multiple nets.
- Node Highlighting now highlights a net properly through multiple hierarchy levels.
- Fixed problem where node highlighting used a DRC license, and thus would not run with L-Edit SDL or HiPer SDL packages.
- Interactive DRC now works correctly with some of the rules turned off.
- Fixed problem in Extract where wrong device was extracted.
- Problem in Generate Layers with layer names containing non-alphanumeric ascii printable characters (-, /, etc) is fixed.

- Probing from netlist to layout now supports one and two coordinate devices, allowing probing of parasitic resistors and capacitors from HiPer PX.
- Tech file with skill constructs no longer causes Virtuoso setup to fail.
- Import Virtuoso setup no longer has wrong GDS number when \_ or – is in the layer name. Import Virtuoso also no longer crashes on empty layer names.
- Tools > AddIns > Bias Mask now generates correct patterns when wires are butt end type.

## **What's New in HiPer Verify v14.12**

- Extract now computes correct L and W values when source and drain are connected.
- Fixed problem in Calibre command file syntax checking, where Net Area Ratio Accumulate did not return a polygon object.
- Fixed a case where HiPer failed to extract the netlist.
- Fixed a problem where the OPPOSITE metric for EXT, ENC, and INT was computed incorrectly for the case of one orthogonal and one non-orthogonal edge.
- Fixed problem in netlist when a cellname and device definition have the same name

# Tanner Tools Version 14.11

## What's New in S-Edit v14.11

- Fixed problem where file paths for simulation could not be changed when the user interface language is set to any language other than English.

## What's New in T-Spice v14.11

- There are no new features in T-Spice v14.11.

## What's New in W-Edit v14.11

- There are no new features in W-Edit v14.11.

## What's New in L-Edit Pro v14.11

- There are no new features in L-Edit v14.11.

## What's New in HiPer Verify v14.11

- There are no new features in HiPer Verify v14.11.

# Tanner Tools Version 14.10

## What's New in S-Edit v14.10

### Symbol Generator

- A new symbol generator is available to allowing user specified values for various parameters of a symbol. These include i) which side ports of different types are placed, ii) port size, iii) port spacing, and iv) whisker length. Existing symbols can also be updated with new ports added to schematic. Invoke **Cell > Generate Symbols** to use this feature.

### Hierarchy Printout

- A new hierarchy tree printout is available. Invoke **File > Hierarchy Report** to print the hierarchy of cells used in a single cell, for all cells in the design, or all cells in the design and libraries.

### Cross Probing

- New features have been added to cross probing to jump from an instance in schematic to the corresponding instance with the same name in layout and visa-versa. There are also commands to jump from a net in schematic to a net in layout. Invoke **Tools > Jump to ...** or use the right click menu.

### Printing

- An option to evaluate properties when printing has been added to the Print dialog. This option applies only when printing the active view.

### Bug Fixes

- Netlabels that end in a ! are now converted to global ports and are correctly snapped to wires when importing EDIF. In v14.0x the ports were not snapped correctly, and in v13 they were snapped, but not converted to global ports.
- Copy/paste of a collection of sequentially named instances now preserves the sequence when auto-naming the copies.
- Fixed crash when net is labeled as out<0:0:0>.
- Fixed problem with connectivity views when renaming views.
- Fixed problem where hierarchy navigator loses cell name when Show Hierarchy or Roots/Leaves Icons are toggled.
- The Find command is fixed for Add and Subtract selections. Find is also fixed to zoom to the correct object.
- Fixed problem where designs used scripts in open.design scripts, and S-Edit did not preserve the current directory across the running of the scripts. This led to the relative paths in the libraries.list files failing to resolve correctly.

## What's New in T-Spice v14.10

- New **.assert** command enables Safe Operating Area checks of circuit devices and state variables
- Corrected problems with **.ic** initial conditions for inductors in **.alter** blocks
- Corrected problems with the **.table** command for devices with 2 or 3 terminals

## What's New in W-Edit v14.10

- There are no new features in W-Edit v14.10.

## What's New in L-Edit Pro v14.10

### Temporary Rulers

- A new temporary ruler may be drawn by pressing the “T” key, then moving the mouse. A ruler may be started while in the middle of drawing an object. Pressing the left mouse button places the ruler, pressing the right mouse button or ESC erases the ruler. Temporary rulers that have been placed may be erased by pressing the Clear Markers toolbar button (eraser icon) on either the Node Highlighting toolbar, the Verification Error Navigator, or the SDL Navigator. The size of Temporary Ruler text height may be set in **Setup Application > Rendering**.

### Change 90/45/AA mode while drawing or moving

- While drawing a polygon or wire, the drawing mode can be temporarily modified by holding down the Ctrl or Shift key. While in any drawing mode, holding the Shift key constraints drawing to 90 degrees, holding the Ctrl key constraints drawing to 45 degrees, and holding Shift and Ctrl keys allows all angle drawing.
- Move object can be constrained to a 45 degree angle by holding the Ctrl key. Move can be constrained to 90 degrees using the Shift Key.

### Cell/Instance Name Rendering

- Text size of cell and instance names may now be customized with a minimum and maximum text height, in pixels, using settings in Setup Application > Rendering. The text will not exceed the bounding box of the instance, regardless of the settings.

### Wire Editing

- Existing wires can now be continued with additional vertices. Holding the Ctrl key, then middle-clicking on the endpoint of a wire resumes drawing the wire, rather than just editing it. Once drawing is resumed, the left button adds vertices, the middle button backs up, and the right button finishes the wire.

### Group Operation

- The Group operation now allows the user to select one of 6 locations as the origin of the newly created cell. The 6 locations are the 4 corners of the MBB, the center of the MBB and to location of the origin of the parent cell.

### Create and Increment Multiple Ports

- A feature is added to place multiple ports at one time, with specified spacing and direction, and the ability to increment numerical components in the name. When placing or editing a port, press the Multiple button in the **Edit Objects > Ports** tab.

### Set Delta-X and Delta-Y of Arrays

- The Delta-X and Delta-Y of an array can now be easily set to the width and height of the master cell. This is done by selecting the array, invoking Edit Instance, then press. the "Cell Width" and "Cell Height" buttons on the Edit Instance dialog.

## Interactive DRC

- A new feature called Show Distances has been added to Interactive DRC. When enabled, this feature will show a ruler displaying the distance between the vertical edge pair and horizontal edge pair that are closest to, or most in violation of any rule. If the edge pair closest to or most in violation is non-orthogonal, then a ruler is displayed only for that edge pair.
- A new feature called Prevent Violations has been added to Interactive DRC. When enabled, this feature will prevent edit operations from creating violations of the rules setup in Interactive DRC. This feature is enabled from the Setup Interactive DRC dialog.

## X-Ref Cells

- A new capability to redirect X-RefCells has been added in v14.1. Either all cells or selected cells from a selected library may be redirected to another library. X-RefCells can also be unlinked from their library and made into local cells. Use the Cell > Examine X-Ref Cells dialog to redirect or unlink cells.

## Cross Probing

- New features have been added to cross probing to jump from an instance in layout to the corresponding instance with the same name in schematic and visa-versa. Invoke **Tools > Jump to ....**

## Extract

- Extract now uses node names of internal nets when writing out a flat netlist. A node name alias list can be written to list different net labels in the layout that correspond to the same net.

## LVS

- The M parameter of a subcircuit is now interpreted it as a multiplicity of the object to which it is applied.

## Schematic Driven Layout

- A text filter box has been added to the SDL navigator.
- Ripup all nets no longer rips up checked nets.
- All SDL navigator operations are now case insensitive.

## SDL Automatic Router

- Schematic Driven Layout now contains an automatic routing capability. The router supports any number of layers, with user specified width and spacing rules for each layer. For each routing layer, one can keep routing out of specified regions by drawing polygons representing obstructions over those regions. The user may choose to route the entire netlist, or only selected nets. Incremental routing is supported by allowing nets to be ripped-up and re-routed as needed. Manual routing may be integrated with auto routing by identifying the active net prior to manual routing.

## Bug Fixes

- Node highlighting has been fixed where in many case parts of a net were not highlighted in the presence of arrays.

- Problem where if the user lets go of the shift key during an edit operation, the edit vector no longer ended at the cursor.
- Performance of interactive DRC has been optimized for disabled rules.
- The Load Calibre Results Add-In now sets units to 1e-6 by default, and remembers any new value entered.
- LVS no longer crashes on node names with parenthesis.

## **What's New in HiPer Verify v14.10**

### **Short and Open Circuit Warnings in Verification Navigator**

- HiPer Verify will now display DRC and Extract warnings in the Verification Navigator. Multiple labels on a single net (Short Circuit), same label on multiple nets (Open Circuit), Unattached labels, SCONNECT and STAMP warnings are displayed.

### **Extract as Toplevel or Subcircuit option**

- Extract now has the option to write the toplevel cell as a subcircuit or as the toplevel cell. Writing as a subcircuit will create a subcircuit definition with a .subckt and .ends line for the cell being extracted.

### **Bug Fixes**

- Problem where bad devices reported in Error Navigator and in Summary Report did not match is fixed.
- Fixed crashes in extract occurring under certain circumstances.
- Fixed problem where text labels were not getting attached to nets.
- Fixed crash in NET AREA RATIO with empty layers.
- DRC and Extract Summary Report now includes a section listing hidden layers. Hidden layers are ignored in DRC and Extract.
- Fixed problem where syntax check would hang indefinitely.
- Unsupported options and commands are now parsed and a warning is given indicating that the option is ignored. Warnings are now given for the WITH NEIGHBOR command, for the BY NET option of the CUT, TOUCH, ENCLOSE and INTERACT commands, and the EXCLUDE SHIELDED option of INT, EXT, ENC.

# Tanner Tools Version 14.02

## What's New in S-Edit v14.02

- Fixed problem where the schematic view would not display correctly when pushing into an instance. This occurred when the instance was in a library of the cell in which the instance was placed.
- Fixed problem when EDIF files were imported, the SPICE output had a invalid ")" character after device name.

## What's New in T-Spice v14.02

- There are no new features in T-Spice v14.02.

## What's New in W-Edit v14.02

- There are no new features in W-Edit v14.02.

## What's New in L-Edit Pro v14.02

- There are no new features in L-Edit Pro v14.02.

## What's New in HiPer Verify v14.02

- There are no new features in HiPer v14.02

# Tanner Tools Version 14.01

## What's New in S-Edit v14.01

- Fixed problem where Keyboard Shortcuts were not properly saved. Newly assigned Keyboard Shortcuts were lost after S-Edit was restarted.
- Problem with the Delete page function deleting all the contents of another page is fixed.
- Properties are now exported with correct type when exporting VHDL.
- Fixed problem where bus signals were reversed in Verilog exported netlist when net labels were used.
- Fixed problem where zero size Port Instances slowed down hierarchy traversing and design save.

## What's New in T-Spice v14.01

- Corrected the behavior of the .measure command when the rise, fall, or cross value was set to "last".
- Changed the PWL source waveform REPEAT behavior. Previously the repeat value would signify the end of the repeated time length, and now it signifies the start of the repeated portion. e.g. for a 100ns PWL wave and REPEAT=60ns, T-Spice will now repeat the 60ns - 100ns portion of the waveform, rather than 0 - 60ns.
- The performance of the .probe command was degraded in release 14.00, and has been improved.
- Mutual inductors in subcircuits were previously failing due to unresolved inductor names, and are now correctly identified within the subcircuit hierarchy.
- Added a warning message if the .connect command is used to rename global GND.
- Performance improvements have been made in the setup phase of Verilog-A devices.
- Input error messages sometimes listed an incorrect input file line number.
- The optional filename parameter in the .print and .probe commands will now be located relative to the output file path, rather than the input file path.
- Fixed problem where some Verilog-A operations fail when multi-threading, causing a crash.
- Improved error message when a subcircuit and a Verilog-A module both use this name. This is not allowed.

## What's New in W-Edit v14.01

- There are no new features in W-Edit v14.01.

## What's New in L-Edit Pro v14.01

- Fixed a bug in the Duplicate operation, where if the starting point of the CTRL-LMB is not on the object corner, then the placed object is incorrect.
- If user changes the layer of an object in the Edit Object dialog, and does not modify the datatype, the datatype of the object will now be automatically set to the datatype of the target layer.
- Fixed problem where Select Edge of a polygon crashes 64-bit L-Edit.

## **Extract**

- Fixed problem where the Capacitance value of a Capacitor Device was incorrectly calculated as zero when the RLAYER of the device was a drawn layer.
- Fixed problem in Standard Extract where two devices with same RLAYER but different PIN layers are not extracted.

## **What's New in HiPer Verify v14.01**

### **Calibre® Compatible DRC**

- Implemented the INSIDE OF layer option for net area ratio.
- Fixed calculation of equality to zero for EXT.

# Tanner Tools Version 14.00

## Tanner Tools 64 bit

Tanner Tools is now available in a 64 bit release enabling significantly larger design sizes to be operated upon. Designs saved in 32 and 64 bit versions are interchangeable.

## What's New in S-Edit v14.00

- The Find feature in S-Edit now supports case insensitive search, wildcards, and regular expressions.
- When importing Cadence schematics, S-Edit now import interface ports and net labels that end with '!' as global ports.
- Verilog instance names that contain [ or ] now have those characters rewritten to < and >, respectively.
- Pin type is now imported from CDL via the .PININFO command.
- Changed processing of subcircuit ground pins - if any .subckt pin name is one of the names for ground (0, gnd, gnd!, or ground) then all ground references in the subcircuit will be aliased to that pin.
- A new EDIF Export option is provided to flatten a design containing multiple libraries, and Export the EDIF as a single design with no libraries.
- All fields in the Simulation Setup dialog are now evaluated. This allows customization of settings, such as setting the output filename based on the name of the cell being simulated. Pathnames in this dialog should now use forward slashes.
- The SPICE.ORDER property can now be a double.
- Properties of type integer are now able to support expressions
- S-Edit has been upgraded to use TCL v8.5.
- In the Import Verilog dialog, two fields are added to specify the names of the TieHigh and TieLow cells. These cells will be connected to logic 1 and logic 0 respectively.
- In EDIF import, a new option called "simInfo key" is added when translating Cadence cdsParam properties. This option tells S-Edit which simulator in the cdf file to choose for formatting of netlist output, as given by cdfld->simInfo in the cdf file.

## Bug Fixes

- Fixed a problem where activating a window would cause it to become maximized.
- Performance of pop-context is significantly improved
- Problem with global ports in arrays is fixed. Ground ports in arrays are now correctly shorted.
- Fixed problem where S-Edit could not load a library if the library name contained a space.
- Export EDIF will now include libraries that are added but not used in the design.
- Fixed problem where a procedure in a namespace procedure that use [database instances] would fail when used as a validation script.
- Fixed problem where Cadence cdf were not correctly imported from files in subdirectories.
- Fixed problem with missing cells on Verilog import.
- Verilog import now handles \r and no longer treats \r as return.
- Fixed problem importing Verilog with duplicate module definitions. Duplicates are ignored with a warning.
- Assignment of bus components in Verilog import is now supported.
- Spice import now correctly connects global pins of instanced subcircuits.
- Fixed problem in CDL import where the contents of a subcircuit definition was missing.

- Fixed problem where the port instance was being used from a library setting rather than the primary design setting, causing wires to disconnect from the port box.
- Autogrid calculation has been improved.
- Fix problem where libraries were saved in the current working folder rather than the project folder when the EDIF import was done into a design with an existing view.
- Fixed problem in displaying the frame
- Leading underscore now allowed in IsLegalSPICEnodename validation script.
- Fixed a problem in Design Check where properly connected wires would be falsely labeled as dangling.
- Fixed a problem in Design Check where warnings for Port mismatch between symbol/schematic were swapped (warnings 32 and 33).

## What's New in T-Spice v14.00

- Updated all Philips models (Mextram, Mos20, Mos30, Mos9, ...) using the latest SiMKit version 3.2 code
- Changed the log(), log10(), and log2() functions to solve: (sign of x) log( |x| ), with a warning message if x is negative
- Reduced the overall memory requirements by compacting into one model all transistor models that are exactly equal
- Modified how character strings are entered for subcircuit, device, model, and .param string parameter values. New option STR (.option str=true|false|0|1, default value: true) controls whether string parameters must be entered using str("...") syntax (the default) or using double quotes. i.e. .param name=str("value") or .param name="value".
- Changed processing of subcircuit ground pins - if any .subckt pin name is one of the names for ground (0, gnd, gnd!, or ground) then all ground references in the subcircuit will be aliased to that pin.
- Verilog-A compiler has been upgraded to release 1.75, correcting several bugs and adding new features such as array arguments to analog functions.
- Resistor's AC resistance value will be limited using the **minresistance** option value (default 1e-5 Ohms).
- Implemented new resistor flicker noise equation and parameters: **ef** (frequency exponent, default value 1.0 ), **lf** (effective length coefficient, default value 1.0), and **wf** (effective width coefficient, default value 1.0).  $F_n = k_f * L_{eff}^{lf} * W_{eff}^{wf} * I_{ds}^{af} / Freq^{ef}$
- Added Cgs, Cgd, Cdtot, Cgtot, Cstot, and Cbtot gate and total capacitances to the BSIM3 and BSIM4 AC small-signal parameters.
- Added support for the combination of voltage-controlled resistors with model definitions.
- BSIM4 models have been updated to include the latest BSIM4 v4.6.2 and v4.6.3 releases.
- Changed the default value of option **prtinterp** to true, so that **prtdel** timepoints are interpolated rather than computed.
- New options **probetop** and **probelvl** are available for limiting .probe and .print output to certain levels of subcircuits: probetop sets the lowest level of subcircuit hierarchy that will be printed, and probelvl sets a specific level.
- External C model support is available in 32-bit, but not 64-bit, T-Spice. Support for external C models will be discontinued in T-Spice version 15, and users are encouraged to convert C models to Verilog-A.
- New option ModMonte=(true|false), default: false, allows transistor model parameters to be varied per device during Monte Carlo parameter sweeps. Use Modmonte=1 for device-level MC analysis, and Modmonte=0 for lot-level MC analysis.

## Bug Fixes

- Made some corrections to the diode capacitance equations when parameter dcap=2
- Fixed a bug when AKO models are used with .alter blocks, and the underlying models are changed.
- Corrected some crashes in various device template (aka device detail) plots.
- Corrected a problem where model parameters that are equations of Monte Carlo variables were not displayed in the output listing of Monte Carlo parameters. Also improved the display of MC variable statistics.
- Corrected problems when reading SPICE statements that include unusual combinations of blank lines, comment lines, and continuation lines.

## What's New in W-Edit v14.00

- There are no new features in W-Edit v14.00.

## What's New in L-Edit Pro v14.00

- A command has been added to draw a guard ring around the mbb of the selection. Previously, guard rings could only be drawn around the perimeter of a selection.
- Improved import of Laker Setup into L-Edit and improved warnings for unknown commands.
- Fixed problem where turning on Merge option in Generate Layers dialog would cause an error.

## Precompiled UPI Macros and T-Cells

- UPI Scripts and T-Cells are now precompiled as DLLs in the background and then executed, rather than being interpreted. UPI scripts can also be explicitly saved as DLLs and loaded later for use. Developers of UPI macros can therefore easily save their macros in DLLs for distribution to users. Example macros have been updated to compile correctly with the new compiler.
- C++ can now be used in UPI scripts and T-Cells as the compiler fully supports C++.
- By precompiling macros and T-Cells there is a onetime penalty in performance the first time the macro is used for improvements in performance on subsequent usage.

## Geber Import/Export

- This Add-In can import a RS-274D or RS-274X Gerber file into L-Edit. You can also export your layout as a Gerber file. Gerber Import/Export requires an add-on license, which can be purchased separately. For more details, please call Tanner EDA Sales toll free at 1-877-325-2223 or 1-626-471-9700 or email [sales@tanner.com](mailto:sales@tanner.com).

## WaferTools

- WaferTools provides the ability to label all die on a Wafer either sequentially or with its row and column. It can also populate a wafer with die maximizing the total number of die on the wafer and handles keep-out regions. WaferTools can sort a group of die based on whether they inside, outside, or on boundary of the Wafer. There is also options to trim layers to the boundary of the wafer. WaferTools requires an add-on license, which can be purchased separately. For more details, please call Tanner EDA Sales toll free at 1-877-325-2223 or 1-626-471-9700 or email [sales@tanner.com](mailto:sales@tanner.com).

## SDL

- SDL now removes device designators such as M, D, Q, R, C when the option "Remove device designator for instance names" is checked. Previously only X was being removed.
- A new option "Insert Multiple devices where M > 1" is added to the Import Netlist dialog. Here M is the multiplicity parameter on a device. Checking this option will cause M separate instances of a device to be placed, rather than a single device with multiplicity M.

## LVS

- Flattened Netlists written by LVS now use the @ symbol instead of parenthesis to designate hierarchy in device and net names. For example M1@X1/X2/ for devices and N1@X1/X2/ for nets instead of M1(X1/X2/) and N1(X1/X2/). The new format is compatible with T-Spice and H-Spice.
- Duplicate subcircuit definitions are now ignored, with a warning.
- LVS now supports the .CONNECT command to short two nodes. The syntax can be in the form of either ".connect C1@X1/ C2@X1/", ".connect X1/C1 X1/C2", or ".connect C1(X1/) C2(X1/)".

## XrefCells

- "Xref cells may now be unlinked from their libraries. Use Cell > Examine XrefCells..., and use the "Unlink" button in the Examine XrefCell Links dialog.
- Cell names in the conflict resolution dialog are now sorted alphabetically.
- Left-dragging from Design Navigator of one design to Design Navigator of another design now does a copy instead of a move. In the Copy-cell dialog, the default radio button is changed from Move to Copy.

## Bug Fixes

- Virtuoso import now uses a real LISP parser to process its input, fixing many problems in Virtuoso import. The "s-expression" form of commands "(command ...)" and prefix form of commands "command(...)" now both work.
- Fixed problem in decoder T-Cell example when pitch is small.
- Wire utilities now respect the locked cell status.
- DRC-box and Verification Navigator now work correctly while editing-in-place.
- In Node Highlighting, fixed erroneous error message : "Database resolution must be at least 10 internal units per technology unit to run node highlighting" when problem was actually a write permission problem.
- Fixed bug in offset of "Duplicate" operation.

## What's New in HiPer Verify v14.00

### Assura® Compatible DRC

HiPer Verify provides a significant advancement in v14 with the support of Assura DRC. SKILL commands that control the flow of the DRC checks are also supported, so the command file may be run directly in HiPer Verify without modification. Layer names/purposes and parameters imported via L-Edit's Import Virtuoso Setup will be used when running Assura command files. Assura support is currently in Beta release.

## Calibre® Compatible DRC

### Antenna Rules and CONNECT optimization

- Many problems that affect Antenna rules and connectivity optimization (CONNECT, SCONNECT, STAMP) have been fixed. Performance improvements in Antenna Rules have also been made.

### Bug Fixes

- The summary report now shows all rules that were run and all rules that were turned off. Rules enabled or disabled by DRC SELECT CHECK and DRC UNSELECT CHECK are correctly shown in the summary report.
- Fixed false errors in spacing rule.
- False syntax checking violations are fixed.
- Problem in the STAMP command has been fixed. This was producing errors in Extract when "Save node highlighting data" was checked.
- Fixed problem where via layer connectivity was not being properly attached when the only connectivity based operation that used the connectivity was an SCONNECT operation.
- The dialog warning that layers are hidden when running DRC or Extract now has a button to "show all layers and start".
- Fixed a problem in Extract that issued Internal Error #5 due to incorrect layer merging.
- Fixed bug in NOT COINCIDENT EDGE command.
- Problems handling certain hierarchy in Extract are fixed. Extracting flat and hierarchical layout would give different results. Now both give the same correct results.

## Calibre® Compatible Extract

### Bug Fixes

- Fixed bug in which nmos devices were being unnecessarily flattened.
- Extract no longer promotes nets that are internal to a subcircuit up to the subcircuit interface.
- Fixed problem where turning on node highlighting with Extract would produce incorrect netlist.

## What's New in HiPer PX v14.00

- There are no new features in HiPer PX v14.00.

## What's New in Tanner EVI v14.00

- Tanner EVI is now working properly. The communication to EVI had broken in v13.14.

## File Associations

- The way file extensions associate with Tanner software has changed in v14. The previous behavior in which running any version of Tanner software would change associations to that version is no longer present. After installing v14, file extensions are always associated with v14 software until another version is installed. For example, installing v14 then running and closing v13, and then double-clicking on a tdb file will launch v14 rather than v13. Switching between v14 and earlier versions

may also corrupt icons. Running the v14 software or reinstalling the desired version of the software will fix any association problems.

- Certain problems with file associations have been fixed. Double-clicking a file saved on the desktop will now open the file correctly. Double-clicking to open a file on Windows Vista 64 now works correctly. This fix applies to all applications, not only to tdb files.

# Additional Information

## Minimum System Requirements

Microsoft® Windows XP or Windows Vista™  
Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support  
512 MB RAM  
425 MB of available disk space with an additional 100 MB during installation  
A video card with at least 64 MB of memory  
3 button mouse

## Recommended System Requirements

Microsoft® Windows Vista™ 64  
Dual Core Intel® Xeon® 2.66 GHz or better processor for desktops  
Intel® Core™ 2 Duo 2.00 GHz or better processor for laptops  
4 GB RAM  
1 GB of available disk space with an additional 100 MB during installation  
A video card with at least 256 MB of dedicated memory  
Microsoft® Intellimouse  
1280 x1024 Resolution - True Color (24-bit)

## Installation

Install Tanner Tools from the Windows operating system. To begin, insert the distribution CD into your CD-ROM drive. The setup program should start automatically; if it does not, then you should navigate to the main CD directory from a file browser window, and double click SETUP.EXE to run setup. The Tanner Tools setup program will provide information on how to proceed.

Administrator Privileges are required to install Tanner Tools v14. Power users are no longer able to install Tanner Tools, as they could in previous versions.

On some Windows Vista machines, the following error will appear when installing, even if you are logged in as an administrator: "Error 1925. You do not have sufficient privileges to complete this installation for all users of the machine. Log on as an administrator and then retry this installation." If this occurs, the right-click on setup.exe on the installation CD and select option Run As Administrator. This will bring you Tanner Setup window and the installation will proceed.

Starting Tanner programs from the Windows Start menu, when logged in as a different user than the user who performed the installation, will sometimes result in a message from Windows requesting insertion of the installation CD. Inserting the CD and following the instructions will complete the installation for this user, and the message will not appear again.

If you install just T-Spice and want to run Verilog-A, you must also install Minimalist GNU for Windows using Custom Installation.

## Licensing

Tanner Tools is licensed software; to use the program, you must have a license from Tanner Research, Inc. Tanner Tools will verify the license either from License Server, installed on your company network, or from a hardware lock attached to your computer's parallel port. Tanner Tools is available in node- or network-locked licensing.

When using the **Interlink** or **LapLink** utilities over the same port as the Tanner Research **Sentinel C-Plus-B** hardware lock, the user must first remove the hardware lock from the parallel port. This must be done in order to keep the Sentinel C-Plus-B lock functional.

This version of Tanner Tools uses the SentinelLM version 7.3.0.6 License Server.

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