

# Tanner Tools v15.02 Release Notes

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# Tanner Tools Version 15.02

## What's New in S-Edit v15.02

- When exporting Spice, quoting of expressions containing spaces is now handled correctly.

## What's New in T-Spice v15.02

- Fixed noise plot items - inoise(m), inoise(db), inoise(tot), etc.
- PWL sources can now accept a single point in the pwl vector.

## What's New in W-Edit v15.02

- W-Edit now loads tsim files correctly when the simulation results folder has Japanese characters.
- In Japanese UI, changing Spice Simulation > General > Show Waveforms to "{Don't show}" no longer gives an error.

## What's New in L-Edit Pro v15.02

- When exporting GDSII with the option Overwrite object data type with layer data type" set, a warning is now issued if the layer data type is blank.
- When importing a Spice netlist into SDL, SDL now correctly instances X-Ref cells containing T-Cells.

## What's New in HiPer Verify v15.02

- VIRTUAL CONNECT COLON is now supported in HiPer Extract.

# Tanner Tools Version 15.01

## What's New in S-Edit v15.01

- On Verilog import S-Edit now issues a warning when case-insensitive name collisions occur, for nets and for instances.
- A problem with corruption of instance names on Verilog export is fixed.
- A problem where instances would show some parts as selected is fixed.
- In Setup Simulation, a new sweep type named <disabled> has been added for DC and Parametric Sweeps, to enable a particular sweep to be disabled.
- Custom Settings in **Setup Technology** can now be saved correctly into the project folder.
- S-Edit will now check if a design has been modified by another user prior to saving, and will give a warning and not save if the design has been modified.
- Added an option "Exclude instance locations" in Spice Export to suppress writing of the instance locations.
- S-Edit can now print to printers other than the default printer.
- Current probing on subcircuits now shows Mag and Phase, same as when probing primitive devices.
- Fixed problem where Design Check was reporting an incorrect number of errors and warnings.
- Fixed problem with the Display.WhenNotEvaluated property to correctly display current annotations.
- Fixed problem where print with Selected Design/Libraries is printing out duplicates causing more printed pages than necessary.
- Fixed problems with Jump > Device in Schematic and Jump > Net in Schematic, when jumping from devices and nets in a netlist to schematic.
- Fixed incorrect results in Spice export in certain circumstances when using net caps.
- Added a new checkbox to Open Design, called "Open design for writing, and libraries read-only". Here "Open as read-only" does not mean "don't write", rather it means "do not grab a lock (i.e. a write-reservation)".

## What's New in T-Spice v15.01

- Added support for encryption of T-Spice netlists using .protect and .unprotect commands combined with the **File > Encrypt...** command.
- Corrected external C device terminal connections error test, which was sometimes issuing incorrect error messages.
- The numerical format of .measure command outputs are now controlled by the **ingold** option: 0=engineering notation and 1=scientific notation.
- Added support for g element (VCCS) and h element (CCCS) M multiplicity parameter, which inherits through the subcircuit hierarchy.
- Limit the amount of repeated error message printouts, using option MAXMSG to set the limit.
- Improved fault tolerance for controlled-source expressions that may result in a 'divide by zero' error.
- Corrected the .measure **pp** peak-to-peak calculation
- Added limits to the Monte Carlo log messages, and send output to the new \*.monte output file.
- Changed the default setting for **.option csv=[012]** to 0, to disable generating the \*.csv comma separated value file.
- Corrected a bug where node names containing a colon were truncated to just those characters following the colon.

- Diagnosed problems compiling Verilog-A code on a network drive: Windows UAC (User Account Control) must be disabled. Please contact support for further information if you are unable to compile modules that are stored in network files.
- Ensured that the plot command `i(deviceName)` is equivalent to `i1(deviceName)` for all devices and all output commands (`.print`, `.measure`, `.assert`, etc.)
- Modified the syntax for conditional statements in expressions (`c ? a : b`) to not necessarily require spaces surrounding the `?` and `:` characters.
- Corrected some circumstances where a column 1 '+' continuation character caused errors within expressions.
- T-Spice now treats “ \$ “ as an end of line comment in P-Spice mode.
- Various performance improvements relative to T-Spice v15.00

## What's New in W-Edit v15.01

- Cross probing of AC simulations now works correctly.
- Added a new tcl command `measure cursor -cursor xxx` to return the x position of vertical cursor named xxx or the y position of a horizontal cursor, as a real number.
- Fixed problem where `.alter` variations were being combined into a single `.alter` in the variations browser.
- MeasureAt now returns the correct result.

## What's New in L-Edit Pro v15.01

- Fixed crash clicking Cell Width button when multiple instances selected.
- `position`, `moveorigin`, `locate`, `layer`, `save`, `database cells`, `database xreffiles`, `database layers`, `property get`, `property set`, `property delete` now operate in T-Cells. Previously, they only operated on the visible cell.
- Auto-panning now works correctly for all objects, regardless of mouse button state.
- **Add selection flyline** now works with HiPer DevGen T-Cells.
- Fixed “Out of memory” error in node highlighting by handling circles correctly.
- Importing a netlist in SDL now first checks the Additional XRef Libraries in the SDL Import netlist dialog, then checks the XRef files in Setup > Design > XRef files, in the order they are listed.
- Note: If problems occur in writing the user `ledit.ini` file, as a work around on Windows Vista and Windows 7 one can turn off User Account Control (UAC), or move the file out of the programs folder to a data folder.

## DRC

- The **Ignore Acute Angles** option now works correctly in L-Edit/DRC.

## What's New in HiPer Verify v15.01

- Problem loading DRC results when multiple rule files are run is fixed.
- Running a single rule now only computes connectivity if necessary. In previous versions, when DRC INCREMENTAL CONNECT was set to YES, then connectivity would always be computed when running a single rule.
- False errors in Net Area Ratio are fixed.
- Problem in calculation of `ABUT ==90` option in DRC rules is fixed.
- Fixed **Jump to DRC Rule** for SCONNECT violations.
- Fixed problem parsing “Inside of Layer” option of RECTANGLES operation.
- Improvements are made in the removal of duplicate operations in command files.
- Improved parsing of Calibre command files to recognize new commands.

# Tanner Tools Version 15.00

## What's New in S-Edit v15.00

### Spice and Verilog-A Text Views

- S-Edit now supports Spice and Verilog-A text views. Any combination of i) schematic, ii) Spice, and iii) Verilog-A view may be saved for a cell. The view that is used when simulating is given by a priority list of view types and view names defined in the Hierarchy Priority tab of the Setup Simulation dialog. A similar list is on the Export Spice dialog for use when exporting Spice.

### Spice Command Tool

- The Spice Command Tool for inserting new Spice commands is now available in the **Additional Spice Commands** page of the **Setup Simulation** dialog. The **Insert Command...** button is used to invoke the wizard.

### Model Parameter Listings

- A table showing all the models supported in T-Spice is now available in S-Edit via the **Help > Models Supported by T-Spice...** menu. A table showing the models used in the libraries specified for the current design is available via **Tools > T-Spice Library Models**, and a table showing the device parameters for all devices in the design is available via **Tools > T-Spice Device Parameters...**. The Help > Models Supported by T-Spice table shows default values for all models and devices, whereas the Tools menu shows tables with the actual models and device values to be used in the simulation of the current design.

### Design Checks

- Performance of design checks has been significantly improved. A limit of 20 errors are reported for each design rule.
- A new design check for checking overlapping wires has been added.
- The default severity of "illegal connectivity" design checks, such as connecting buses of different widths, is now Error instead of Warning.
- The design check for overlapping instances now ignores symbols that do not have any ports. This prevents the design check from flagging frame instances, which overlap the entire schematic.
- Design check now performs cell name checks in a case insensitive manner. Cell names in different libraries with same name but different case will now issue a warning/error.

### Bug Fixes

- Performance of Push and Pop context is significantly improved.
- Design checks now properly identifies the case when two cells with same name are instanced from different libraries.
- Fixed problem when importing an EDIF schematic file created in S-Edit, the option "Overwrite existing views" did not work properly.
- S-Edit has a new Simulation Setup option, "Keep all simulation results". When True, a time stamp is appended to the Simulation Results folder, so each simulation is saved in a unique folder. When False, prior results are overwritten.

- Fixed problem where Verilog import would have missing pins when a module definition contains a port, but does not declare the port in the module's contents. These ports will now be declared as type "other" and a warning will be issued.
- Verilog import now imports parameters.
- Ports containing buses with {} brackets now import properly.
- Verilog Import dialog no longer reverts the TieHigh cell: value to TieHigh even when something else is specified.
- Fixed a problem where Property set would apply to selections that were not on the active page.
- Selecting properties on symbols will now select the property that is clicked on. Using the left mouse button will cycle through overlapping properties, allowing one to select difficult to select properties.
- Fixed a problem where a box width could not be changed to be greater than 66 inches.
- An option "Exclude simulator commands" is added to the Spice Export dialog to suppress simulation setup commands during Spice export.
- "New properties \${PageNumber} and \${Pages} have been added. \${PageNumber} evaluates to the 1-based index of the page that contains the instance. \${Pages} evaluates to the total number of pages in the schematic view that contains the instance.
- Zoom to selection now works correctly on highlighted nets
- ORCAD EDIF files may now be imported and the netlisting commands are correctly translated for exporting Spice.
- "Author (renamed from "Creator"), Version, Modification Date ("Last Modified"), Info and Organization and RevisionCount are now included as column choices in the View Navigator.
- Import of Cadence EDIF files now reads callbacks from the cdf file and places the function name and parameters on the property. A tcl file with stubs for the functions is created for the user to provide the content of the tcl function.
- Problems importing EDIF written by the Gateway Schematic Editor are fixed.
- Tcl scripts saved from S-Edit and placed in the user preferences startup folder will now properly load on program startup.
- Exported netlists are now sorted within each sort order block. The sort first sorts the alphabetic characters and then sorts any numbers in the name as a number. For example, the sort will produce C1, C2, C10, C11, whereas a normal alphabetical sort would be C1, C10, C11, C2.
- Printing will now print all pages of a schematic view, rather than just the first.
- In Setup SPICE Simulation, the Verilog search path is now saved.
- When separated by a space instead of a comma, negative values in temperature sweeps were being evaluated as an expression. The description field has been enhanced with: "Use commas to separate negative numbers or expressions"
- Annotations on schematic are now updated automatically after each simulation. It is no longer required to turn off then back on annotations to update after a simulation.
- The InstanceName property on a symbol can now be used as a prefix to use for the instance name when creating a new instance. If InstanceName is "M" then instances will be named M\_1, M\_2, etc. If InstanceName is blank, then the cell name is used.

## Known Issue

- When v15.00 is installed over v14.13, hotkeys don't appear for all items in the Edit menu when a text document is active, although they do function correctly. A workaround is to open the Customize dialog on the toolbar context menu, go to the Keyboard tab, and click the Reset All button. This will restore the shortcuts to the menu, but will undo any custom keyboard shortcuts you have configured.

# What's New in T-Spice v15.00

## T-Spice Model Parameter Listings

- A table showing all the models supported in T-Spice is now available in S-Edit via the **Help > Models Supported by T-Spice...** menu. The table shows the parameters and their default values for all models supported by T-Spice.

## Miscellaneous

- VBIC 3 terminal devices are now supported; 4 terminal VBICs remain as before.
- The `.assert` command can now be used to monitor Verilog-A device terminal currents.
- Binned model naming convention, where the name consists of a trailing period and number (e.g. `nch.1`), now additionally allows a trailing period without a number (`nch.`).
- `.print` output is now written to a CSV (comma-separated value) file as well as the binary database. CSV files can be easily loaded into spreadsheets and other applications. CSV output is controlled with the new option `csv=[0 | 1 | 2]`, 0: disable, 1: store `.print` outputs (default), 2: store `.print` and `.probe` outputs.
- The TC1 and TC2 parameters are now supported for all types of capacitors and resistors (voltage-controlled, polynomial, etc.)

# What's New in W-Edit v15.00

## Completely New W-Edit

W-Edit has been completely rewritten for Tanner Tools v15, and features significant improvements over the previous version.

- **Waveform Calculator:** W-Edit v15 provides a calculator for creating and evaluating expressions involving traces or measurements. The calculator provides trig, and hyperbolic trig functions, exponentiation and logarithmic functions, complex number functions, and mean, median, and standard deviation functions. The calculator provides a platform for easily creating arithmetic traces.
- **Measurement Platform:** W-Edit v15 is not only a waveform viewer, but is an analysis platform featuring built in measurements that can be applied to selected traces. These include `amax`, `amin`, `amplitude`, `average`, `baseline`, `compare`, `cross`, `delay`, `derivative`, `edgethreshold`, `error`, `falltime`, `frequency`, `integral`, `intersect`, `maximum`, `minimum`, `nexctedge`, `nextextreme`, `nextpoint`, `overshoot`, `period`, `previousextreme`, `previouspoint`, `pulsewidth`, `risetime`, `rms`, `slewrates`, `smooth`, `topline`, `undershoot`, `window`, `xval`, `ymin`, `yval`.
- **Arithmetic Traces:** W-Edit v15 supports an ability to create new traces from arithmetic expressions of other traces. Arithmetic traces can be used in expressions or other arithmetic traces. Arithmetic traces can be saved in the W-Edit chartbook.
- **Multiple Simulations:** W-Edit v15 supports loading and viewing of multiple simulations. Results of multiple simulations can be plotted together for comparison and measurements.
- **Programmable:** W-Edit v15 is fully programmable with tcl, allowing the user to write scripts to automate results analysis.
- **Performance:** W-Edit v15 is a high performance waveform viewer able to handle your largest datafiles with ease. The trace navigator is able to display traces in a flat or hierarchical view, with filters including wildcards and regular expressions.
- **Chartbooks:** All configuration aspects of a chart, including arithmetic traces, can be saved to a chartbook for later display.

- **Intuitive GUI:** Drag-and-drop traces onto a chart. Easily view results of parameter sweeps on a single plot, and show/hide results of selected sweeps. Take measurements with multiple cursors.
- **Backward Compatibility:** v14 simulation databases can be converted to v15 format using Wavetool.

## What's New in L-Edit Pro v15.00

### Dev-Gen

- Dev-Gen, the device generators for mosfets, resistors, capacitors, diodes, and inductors has been rewritten with an improved setup and now uses T-Cells, rather than simply placing polygons. As T-Cells, the parameters of devices placed by Dev-Gen can now be edited.

### HiPer Dev-Gen

- HiPer Dev-Gen is a new module of advanced layout generation macros for current mirrors and differential pairs, providing substantial time savings for laying out these complex devices. Mosfets, resistors, and capacitors are also included in HiPer Dev-Gen. HiPer Dev-Gen macros can be instanced as T-Cells in the same manner as standard Dev-Gen T-Cells. Schematic Driven Layout (SDL) is also able to automatically recognize primitive transistors configured as current mirrors and differential pairs, and to place the appropriate T-Cell for that device.

### Import Calibre into Interactive DRC

- Calibre® rule files can now be imported into online DRC.

### SDL Placement

- SDL now uses the schematic placement as a guideline for placement of instances when importing a netlist. This is an improvement over the previous behavior of simply stacking instances in a column.

### SDL Automatic Routing

- The SDL automatic router now supports single layer routing. This is most successfully used in a river routing situation in which one is routing a bus with no crossover of nets, and all pins are on the desired layer, although breakouts are allowed to route from pins that are not on the target layer.
- The SDL router now supports double vias. Create a cell that has a double via in it, then use that cell as your via cell in SDL Router setup.

### Extract

- Extract is now able to label devices by placing port objects at the location of each device. The text of the port is the name of the device.
- Extract now writes device and node counts into the netlist. For a hierarchical netlist, device and node counts are written for each subcircuit, and for a flat netlist the total node and element count is written.
- A new option, BY\_NET has been added to the device definition in the standard Extract definition file. This option counts multiple pins of the same layer that are connected to the same device as a single pin of the device.

## Bug Fixes

- Interactive DRC now works correctly with multi segment wires.
- Two command-line options are added to L-Edit, S-Edit and W-Edit:
  - t <filename> --- causes that tcl file to be 'source'd
  - T <commandname> --- executes the Tcl command <commandname>
- DXF import/export can now handle the ^ character.
- CTRL+ drag box can now select both ends of a wire
- Splines are now imported in DXF. They are sampled as 20-sided polylines.
- L-Edit no longer crashes when dragging a text file onto the Design navigator.
- GDSII Export with lower case option no longer appends \_1 to the cell name.
- L-Edit-64 is now able to save TDB files greater than 2GB.
- Fixed a problem where updating the source code of a T-Cell in an x-Ref cell, and then updating the x-Ref T-Cell, the links to the x-Ref cell would become broken.
- When layers are hidden, running Extract will now bring up a dialog asking if geometry on the hidden layers should be ignored, or shown and used.
- Fixed problems when parenthesis was used in recognition layer names in extract definition file.
- Fixed problem where end of line comment using # would comment out entire line in EXT file.
- Fixed problem where ascii control characters in the Setup DRC Standard Ruleset dialog would cause DRC to not report any violations

## What's New in HiPer Verify v15.00

- The Verification Error Navigator is now able to highlight multiple rules at the same time. Click on a rule name to highlight all violations of a rule in the active cell. When violations are sorted by cell first, click on a cell name to highlight all violations of all rules in the selected cell.

## Calibre® Compatible Format

- WITH NEIGHBOR is now supported.
- The REGION CENTERLINE option for INT, EXT, and ENC rules is now supported.
- Netlist Comment Coded Substrate is now supported. If Netlist Comment Coded Substrate is set to YES extract will write three pin resistors, diodes and capacitors as two pin devices with third pin in comments. In set to NO extract will write these devices as a primitive subcircuit.
- 

## Bug Fixes

- EXPAND CELL now correctly expands instances of specified cells one level into the cell in which such instances are placed. Previously EXPAND CELL would completely flatten instances of specified cells. EXPAND CELL also now will match to T-Cells, which have a suffix of \_AUTO\*, and x-Ref Cells, which have a suffix of :LibraryName.
- Fixed checking of the OVERLAP option of ENC command, to make sure that polygons are properly overlapping and not just coincident before performing overlap check.
- Fixed ENC with SINGULAR option which would sometimes give false errors between abutting cells of a hierarchical layout
- Implemented special case handling of ABUT == 0 for ENC, EXT, and INT commands. If the abut constraint includes zero in its range then, for ENC, any edges that are coincident inside are also output, and for EXT and INT, any edges that are coincident outside are also output.

- The OFFGRID command is now able to use an expression in the layer parameter, for example, OFFGRID (A not B) 5
- The SNAP command is now able to use an expression in the layer parameter.
- Fixed a problem where WITH WIDTH command was not considering very thin 45 degree polygons.
- Fixed a problem where expressions inside a NET AREA RATIO command inside a DRC rule were incorrect.
- Fixed problem with rule names containing an "&"
- Fixed a problem when a DRC rule is written using variables in rule comment, the Verification Error Navigator window would only substitute in the first parameter.
- Extract is now able to label devices by placing port objects at the location of each device. The text of the port is the name of the device.
- Extract now writes device and node counts into the netlist. For a hierarchical netlist, device and node counts are written for each subcircuit, and for a flat netlist the total node and element count is written.
- Fixed problem where pins of a device were incorrectly shorted.
- False SCONNECT warnings are no longer reported
- Problems reading in verification errors into the Error Navigator after Extract have been fixed.
- A problem in which the collector and emitter of a BJT were getting shorted has been fixed.
- Fixed crash caused by mismatching case in layer names.
- Fixed syntax checking problem that would cause L-Edit to hang.
- Fixed a problem where a device was identified as a bad device in hierarchical layout, but would be recognized properly when flattened.
- Fixed problem that caused \$\$ TwoLayerPerimeterCalculator: internal error #3
- Fixed problems in hierarchical extraction related to pushing down of devices.

## **What's New in HiPer PX v15.00**

- There are no new features in HiPer PX v15.00.

# Additional Information

## Supported System Requirements

Microsoft® Windows XP, Windows Vista™ or Windows 7.  
Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support  
1 GB RAM  
425 MB of available disk space with an additional 100 MB during installation  
A video card with at least 64 MB of memory  
3 button mouse

## Recommended System Requirements

Microsoft® Windows 7 64-bit  
Dual Core Intel® Xeon® 2.66 GHz or better processor for desktops  
Intel® Core™ 2 Duo 2.00 GHz or better processor for laptops  
It is recommended to get a computer with at least 2 cores and the fastest processor speed you can afford. Tanner Tools can take advantage of 2 cores/processors but not more. It is also recommended to get the fastest RAM you can afford.  
4 GB RAM  
1 GB of available disk space with an additional 100 MB during installation  
A video card with at least 256 MB of dedicated memory  
Microsoft® Intellimouse  
1280 x1024 Resolution - True Color (24-bit)

## Installation

Install Tanner Tools from the Windows operating system. To begin, insert the distribution CD into your CD-ROM drive. The setup program should start automatically; if it does not, then you should navigate to the main CD directory from a file browser window, and double click SETUP.EXE to run setup. The Tanner Tools setup program will provide information on how to proceed.

Administrator Privileges are required to install Tanner Tools v14. Power users are no longer able to install Tanner Tools, as they could in previous versions. On some Windows Vista machines, the following error will appear when installing, even if you are logged in as an administrator: "Error 1925. You do not have sufficient privileges to complete this installation for all users of the machine. Log on as an administrator and then retry this installation." If this occurs, the right-click on setup.exe on the installation CD and select option Run As Administrator. This will bring you Tanner Setup window and the installation will proceed.

Starting Tanner programs from the Windows Start menu, when logged in as a different user than the user who performed the installation, will sometimes result in a message from Windows requesting insertion of the installation CD. Inserting the CD and following the instructions will complete the installation for this user, and the message will not appear again. If you install just T-Spice and want to run Verilog-A, you must also install Minimalist GNU for Windows using Custom Installation.

## Licensing

Tanner Tools is licensed software; to use the program, you must have a license from Tanner Research, Inc. Tanner Tools will verify the license either from License Server, installed on your company network, or from a hardware lock attached to your computer's parallel port. Tanner Tools is available in node- or network-locked licensing.

When using the **Interlink** or **LapLink** utilities over the same port as the Tanner Research **Sentinel C-Plus-B** hardware lock, the user must first remove the hardware lock from the parallel port. This must be done in order to keep the Sentinel C-Plus-B lock functional.

This version of Tanner Tools uses the SentinelLM version 7.3.0.6 License Server.

## Technical Support

Tanner Research, Inc.  
825 South Myrtle Avenue  
Monrovia, CA 91016-3424, USA

Telephone: 1-877- 304-5544 (Toll Free)  
1-626-471-9700  
Fax: 1-626-471-9800  
E-mail: [support@tanner.com](mailto:support@tanner.com)  
Web: [www.tannereda.com](http://www.tannereda.com)

### Japan

Tanner Research Japan K.K.  
Burex Kojimachi 6F  
3-5-2 Kojimachi, Chiyoda-ku  
Tokyo 〒 102-0083  
Japan  
Tel: +81 (03) -3239-2840  
Fax: +81 (03) -3239-2860  
Email: [sales.jp@tanner.com](mailto:sales.jp@tanner.com)  
Web: [www.tanner.jp](http://www.tanner.jp)

### Taiwan

Tanner Research Taiwan, Inc.  
3FB1, No. 1, Li-Hsin 1st Road  
Science Based Industrial Park  
Hsinchu, 300 Taiwan ROC  
Tel: 886-3-666-2112  
Fax: 886-3-666-3697  
Email: [sales.tw@tanner.com](mailto:sales.tw@tanner.com)  
Web: [www.tanner.com.tw](http://www.tanner.com.tw)

### Europe

EDA Solutions Limited  
Unit D, 58 Botley Street  
Park Gate  
Southampton, SO31 1BB  
United Kingdom  
Phone: +44 (0) 1489 564253  
Fax: +44 (0) 1489 557367  
Email: [tanner@eda-solutions.com](mailto:tanner@eda-solutions.com)  
Website: [www.eda-solutions.com](http://www.eda-solutions.com)

### Israel

New Artech Technologies Ltd.  
Kochav Herzeliya House  
4th Floor  
4 Hasadnaot Street  
46120 Herzeliya Pituach  
Israel  
Phone: 972 99 962-8080  
Fax: 972 99 962-8090  
Email: [roniamir@a-r-tech.com](mailto:roniamir@a-r-tech.com)